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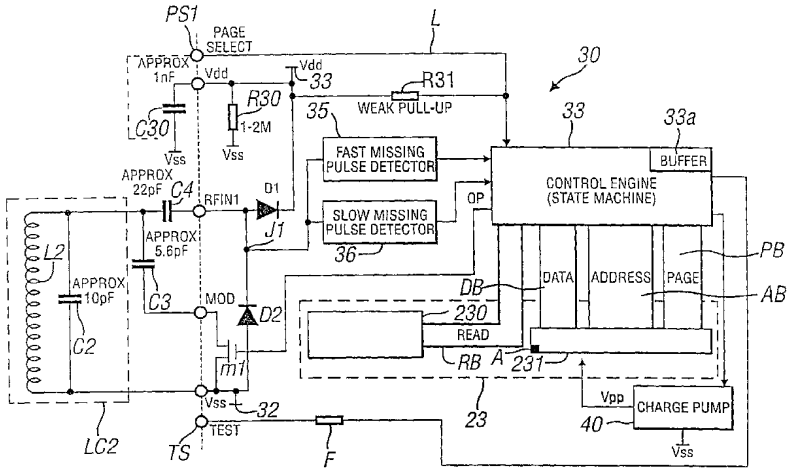
(54) Title: DATA COMMUNICATION APPARATUS



(57) Abstract: A base module (2) has a subsidiary unit receiving area (3b) having a first electrical coupler (LC1). A subsidiary unit (4) has a memory (231) and a second electrical coupler (LC2) arranged to couple to the first electrical coupler when the subsidiary unit is received on the subsidiary unit receiving area (3b). The base module (2) has a signal supplier (10, 21) for supplying a signal to the subsidiary unit (4) when the first and second electrical couplers (LC1 and LC2) are coupled and a data communicator (10, 22) for interrupting the signal in accordance with data to be communicated to the subsidiary unit to provide to the first coupler (LC1) an interrupted signal having interruptions dependent upon the data to be communicated. The data communicator is arranged to send the data as data bits each followed by a confirmation bit and the subsidiary unit has a data returner (33, M1) for modifying the received signal to return the received data as it is received so that each returned data bit is followed by the inverse of the corresponding confirmation bit.

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DATA COMMUNICATION APPARATUS

This invention relates to data communication apparatus comprising a base module and at least one passive data storage device wherein the passive data storage device is arranged to be powered by a signal received from the base module and to communicate stored data with the base module when powered. The present invention is particularly, although not exclusively, applicable to games apparatus wherein the base module comprises a games module and the at least one passive data storage device comprises a playing piece and to industrial uses such as asset tracking.

WO98/24527 describes data communication apparatus wherein a base module and passive data storage device are adapted to couple inductively to one another to enable the base module to supply power for the passive data storage device and to receive data from the passive data storage device. WO 00/31676 describes data communication apparatus wherein the passive data storage device is arranged to derive a power supply from a signal supplied by a base or games module by coupling to a user so as to complete an electrical path via the user back to the games module and to communicate data with the games module when power is thereby derived by the power deriving means from the signal provided by the games modules.

The data communication apparatus described in WO98/24527 and WO 00/31676 are read only systems, that is the data stored in the passive data storage device cannot be altered.

US-A-5517188 describes a programmable identification apparatus wherein a transponder is arranged to be powered by the energy of a transceiver transmit signal generated by a transceiver. The transponder includes a programmable memory element storing a coded sequence which uniquely identifies the transponder. When powered, the transponder generates a transponder signal including the coded sequence stored in the programmable memory element. In the apparatus described in US-A-5517188, the transponder transmits its data to the transceiver by modulating the frequency of a transceiver transmit signal in accordance with the stored code. The transponder described in US-A-5517188 is specifically designed to be reprogrammable to enable the stored unique code to be changed on command. This apparatus also enables the status of a portion of the memory to be changed back and forth between a write-protected and a non-write-protected status dependent upon a control signal supplied from the transceiver. The apparatus described in US-A-5517188 thus is specifically designed to facilitate reprogramming to enable the data stored in the transponder to be changed easily. Although this has some advantages, it does, of course, increase the danger of unauthorised tampering with the content of the programmable memory.

EP-A-0441031 also describes a data communication apparatus. This apparatus is specifically designed for enabling reading of data from and writing of data into electronic tags (passive data storage devices) that are moving relative to an interrogator. The interrogator sends a continuous RF signal to the tag which back scatter modulates the received RF signal with data stored in the tag. The back scatter modulated signals are made up of a first frequency component and a second frequency component twice the first frequency component and one of the first and second frequencies is used to represent a zero and the other to represent a one. Like US-A-5517188, this document is specifically concerned with enabling modification of the data stored in the tag and accordingly is intended primarily to facilitate changing of that data. Again, although this may be desirable in certain circumstances, it does increase the danger of unauthorised tampering with the stored data. In addition, both US-A-5517188 and EP-A-0441031 use relatively complex coding schemes for enabling communication of data between the base module and a passive data storage device.

In one aspect, the present invention provides data communication apparatus having a base module or unit and at least one passive data storage device, wherein communication of data between the passive data storage device and the base unit is effected by interrupting a carrier signal and changing the time period for which the modulation is interrupted in accordance with the data to

be communicated. In an embodiment, a short interruption is used to represent a zero while a long interruption is used to represent a one.

In one aspect, the present invention provides a data communication apparatus having a base module and a passive data storage device, wherein the passive data storage device is adapted to generate a power supply from a signal supplied by the base module, the base module is adapted to communicate to the passive data storage device data to be stored in the passive data storage device and the passive data storage device is adapted to communicate received data back to the base module so that the base module can check whether the data has been correctly received by the passive data storage device. This check may be carried out during the writing procedure and may be synchronised and simultaneous with the data sent.

In an embodiment, the base module is adapted to send an alarm signal to the passive data storage device when it determines that the data has not been communicated correctly and to retransmit the last transmitted block of data to the passive data storage device to overwrite the previously transmitted version of that data.

The present invention also provides a base module for use in any of the aspects set out above. The present invention also provides a passive data storage device for use in any of the aspects set out above.

In another aspect, the present invention provides a writeable passive data storage device having a memory divided into a plurality of different sections, wherein at least one of the different sections is configured so that the data stored therein cannot be modified. In an embodiment said one section is preconfigured during manufacture of the passive data storage device, for example by predefined patterning of the metal layer defining the connections to that section of memory.

In another aspect, the present invention provides a writeable passive data storage device having a memory having a number of sections of different memory type such that one or some of the memory sections may not be available for writing to by an end user, one or some of the memory sections may be available for writing to by an end user but only once, and one or some of the memory sections may be available for writing to many times by an end user. The memory may have any combination of any one or more of these memory types. In an embodiment one memory section is preconfigured during manufacture of the passive data storage device, for example by predefined patterning of the metal layer defining the connections to that section of memory. This section may be, for example, mask ROM.

In another aspect, the present invention provides a writeable passive data storage device having page select means for selecting for writing of data one of a number of different pages or sections of a memory of the passive

data storage device. The page select means may be a page select line that enables programming of a section of memory after the passive data storage device has been produced but before the passive data storage device is placed within a housing to form a subsidiary unit but that cannot be accessed or is left in such a state that the at least one memory section cannot then be written to by a user using a base module.

In another aspect, the present invention provides a writeable passive data storage device having means for write-protecting data stored in the passive data storage device such that, when the write-protection is set, the write-protection cannot be removed. This may be carried out at factory level or later during use of the passive data storage device by an end user or supplier to an end user.

In another aspect, the present invention provides a writeable passive data storage device having a test input coupled to control means of the passive data storage device for enabling erasing of a memory of the passive data storage device even if that memory is write-protected, the test input being coupled to the control means via a fusible link adapted to be fused so as to disconnect the test pin.

In another aspect, the present invention provides a passive data storage device wherein a test input for enabling erasing of a content of a memory of the passive

data storage device is isolated from control means of the passive data storage device by a fused fusible link.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a diagrammatic perspective view of data communication apparatus embodying the invention comprising a base module and a subsidiary unit;

Figure 2 shows a functional block diagram of the base module;

Figure 3 shows a simplified functional block diagram of functional components of the subsidiary unit shown in Figure 1, the subsidiary unit comprising a passive data storage device and accompanying coupler carried by the subsidiary unit;

Figure 4 shows a functional block diagram to illustrate operation of a first or second signal deriver of the passive data storage device shown in Figure 3;

Figure 5 shows a circuit diagram illustrating one way of implementing data transmitting and receiving circuitry of the base module shown in Figure 2;

Figure 6 shows a more detailed block diagram of functional components of the subsidiary unit shown in Figure 3;

Figure 7 illustrates very diagrammatically a data carrying signal supplied by the base module shown in Figure 2;

Figures 8a and 8b illustrate diagrammatically the signals supplied by a fast and a slow missing pulse detector to a control engine of the passive data storage device;

Figure 9 shows an example of a data signal received by the passive data storage device while Figure 10 shows a corresponding output data signal returned by the passive data storage device to the base module;

Figures 11a to 11d show diagrammatic representations of signal structures with Figure 11a showing a general command signal structure, Figure 11b showing a write command structure, Figure 11c showing a write-protect command structure and Figure 11d showing an erase command structure;

Figures 12a and 12b illustrate diagrammatically the signal structure of data read from the passive data storage device with Figure 12a showing the structure of a header of the data signal and Figure 12b showing the overall structure of the data signal output by the

passive data storage device in response to a read command from the base module;

Figure 13 shows a flow chart for illustrating selection of different modes of a passive data storage device;

Figure 14 shows a flow chart for illustrating steps carried out by the base module to write data into the passive data storage device;

Figures 15a and 15b show flow charts illustrating steps carried out by the base module and passive data storage device, respectively, to write-protect data stored in the passive data storage device;

Figure 16 shows a flow chart illustrating steps carried out by the passive data storage device in order to write data into its memory;

Figure 17 shows a flow chart illustrating in greater detail a receive and store data step shown in Figure 16;

Figure 18 shows a flow chart illustrating steps carried out by the base module to read data from the passive data storage device;

Figure 19 shows a flow chart illustrating steps carried out by the passive data storage device during reading of data from the passive data storage device;

Figure 20 shows a flow chart illustrating steps carried out by the base module to enable erasing of the memory of the passive data storage device in a test mode;

Figure 21 shows a flow chart illustrating steps carried out by the passive data storage device in response to an erase command;

Figure 22 shows a functional block diagram of another embodiment of a base module in accordance with the present invention;

Figure 23 shows a functional block diagram of another embodiment of a base module in accordance with the present invention;

Figure 24 shows a circuit diagram of one implementation of the data transmitting and receiving circuitry of the base module shown in Figure 24;

Figure 25 shows a modified version of the circuit diagram shown in Figure 5;

Figure 26 shows a diagrammatic perspective view of another example of data communication apparatus embodying the invention comprising a base module and a subsidiary unit;

Figure 27 shows a functional block diagram of the base module shown in Figure 26;

Figure 28 shows a simplified functional block diagram of functional components of the subsidiary unit shown in Figure 26, the subsidiary unit comprising a passive data storage device and accompanying coupler carried by the subsidiary unit;

Figure 29 shows a more detailed block diagram of functional components of the subsidiary unit shown in Figure 28; and

Figure 30 shows a functional block diagram of another embodiment of a base module in accordance with the present invention.

Referring now to Figure 1, a data communication apparatus 1 comprises a base module 2 having a housing 3 that may be moulded from, for example, plastics material.

Data communication apparatus embodying the invention also includes at least one subsidiary unit. One subsidiary unit 4 is shown in Figure 1. The subsidiary unit has a casing or housing 4a which may be formed or moulded from a plastics material and is, in this example, in the form of a flat block or card. The housing 4a of the subsidiary unit may, however, have a three-dimensional shape and may comprise, for example, a figurine (such as a toy animal or human figure) on a base. Although not shown in Figure 1, the subsidiary unit (the base where the subsidiary unit consists of a figurine on a base) contains a passive data storage device.

The housing 3 of the base module has an upper surface 3a on which is defined a subsidiary unit receiving area 3b. The upper surface 3a of the housing also carries a display (for example an LCD or LED display) 5, a loudspeaker 6 and a power on/off switch 7.

As shown by phantom schematic outlines in Figure 1, a tuned circuit part LC1 is accommodated within the housing 3 beneath the subsidiary unit receiving area 3b. The tuned circuit part LC1 is adapted to couple inductively to a tuned circuit part LC2 (shown in phantom lines in Figure 1) carried by the subsidiary unit 4 to form a tuned circuit to enable, as will be described in greater detail below, the passive data storage device carried by the subsidiary unit 4 to derive a power supply from a signal provided by the base module and to enable communication of data between the base module 2 and the subsidiary unit 4.

Figure 2 shows a functional block diagram of the internal components of the base module.

As shown in Figure 2, the base module 2 comprises a controller 10 that may be, for example, a microprocessor or microcontroller associated with a memory 11 (ROM and/or RAM). The controller 10 is coupled, via conventional interfaces (not shown), to the display 5 and loudspeaker 6. The controller 10 is also coupled to a user interface which, in this example, constitutes the power on/off switch 7. As shown in Figure 2, the

controller 10 is also coupled to a communications interface 8. This communications interface constitutes a port enabling communication between the base module and a personal computer, for example. The port may be adapted to receive a terminal of a cable CB (Figure 1) or may be a wireless communications port (for example an infrared port) for enabling communication with a similarly equipped computer.

The controller 10 is also coupled to data transmitting and receiving circuitry (DTR) 20.

As shown in Figure 2, the DTR circuitry 20 consists of an oscillator circuit (OSC) 21 coupled via a gate 22 and filter circuit 23 to an inductor L1 of the tuned circuit part LC1 which comprises the inductor L1 in parallel with a capacitor C1 and with a variable capacitor VC. The gate 22 is coupled to a gate signal output port GP of the controller 10 so that the controller 10 can control whether or not a signal from the oscillator is supplied via the gate 22. The oscillator 21, gate 22, filter circuit 23 and tuned circuit part LC1 provide, in operation, an oscillating signal which is supplied by the inductive coupling provided by the tuned circuit formed between the tuned circuit part LC1 and the tuned circuit part LC2 to the passive data storage device carried by the subsidiary unit 4 when the subsidiary unit 4 is in the vicinity of the subsidiary unit receiving area 3b. As will be described in detail below, this oscillating signal provides a power supply for the passive data

storage device 30 and interruption of the oscillator signal by a gate signal (GATE) supplied by the controller 10 enables data transmission to the passive data storage device 30.

The tuned circuit part LC1 is also coupled via a demodulator 24, filter 25 and buffer/squaring circuitry 26 to a data input D of the controller 10 to enable, as will be described in detail below, the controller 10 to read data supplied by the passive data storage device 30. As shown in Figure 2, the controller 10 may have a power save output PS for switching off the power supply to certain components of the circuitry (for example the oscillator 21 and buffer/squaring circuitry 26 in Figure 2) that consume relatively high amounts of power when those components are not required.

In the interests of simplicity, the power supply to the functional components of the base module is not shown in Figure 2. Generally, however, this power supply will be a battery power supply although, as will be appreciated by those skilled in the art, power may be supplied to the base module 2 via an AC mains supply and a transformer.

Figure 3 shows a simplified block diagram of the functional components of the subsidiary unit 4. The subsidiary unit 4 comprises the passive data storage device 30 and the tuned circuit part LC2 which, in this example, consists of a parallel connection of an inductor L2 and a capacitor C2 across which is coupled a series

connection of a capacitor C3 and an FET M1. A signal inductively coupled to the passive data storage device 30 via the tuned circuit LC1 and LC2 is supplied via a capacitor C4 to a junction J1 between the anode of a first diode D1 and a cathode of a second diode D2. The cathode of the first diode D1 is connected to a first power supply rail 31 (Vdd) while the anode of the second diode D2 is connected to a second power supply rail 32 (Vss). The capacitor C4 and the diodes D1 and D2 act effectively as a voltage doubler enabling the peak to peak voltage of the received AC or oscillating signal to be used by the diodes D1 and D2 to derive a power supply for the passive data storage device 30 from the oscillating signal inductively coupled to the passive data storage device by the tuned circuit LC1 and LC2. It will, of course, be appreciated that, in the interests of simplicity, the power supply connections to the remaining components of the passive data storage device 30 are not shown in Figure 3.

The remaining components of the passive data storage device 30 consist of a control engine 33 which controls reading and writing of data to and from a memory 34. In this embodiment, the control engine is a state machine having its own memory. At least part of the memory is programmable as will be described below.

A clock signal for the control engine 33 is derived from the oscillating signal supplied by the base module via a first signal deriver 35 coupled to the junction J1.

The control engine 33 extracts data carried by the oscillating signal by using the output of the first signal deriver 35 and the output of a second similar signal deriver 36 coupled to the junction J1. A data output of the control engine 33 is coupled to a control gate of the FET M1 so that, as will be described below, when data is output by the control engine 33 on output line OP, the data switches the FET M1. The loading across the inductor L2 varies in dependence upon whether the FET M1 is conducting or non-conducting causing the oscillating signal to be modulated in accordance with the data output by the control engine 33. The data output by the control engine 33 is extracted from the modulated oscillating signal by the demodulator 24, filter 25 and buffer/squaring circuitry 26 to provide a data input signal to the controller 10 (Figure 2).

In this embodiment, the first signal deriver 35 is a fast missing pulse detector while the second signal deriver 36 is a slow missing pulse detector. As shown in Figure 4, each of the missing pulse detectors consists of a high pass filter/differentiator 300 which receives the oscillating signal from the junction J1 and outputs a high pass filtered and differentiated signal to a monostable timer 301. Each edge of the integrated signal triggers the monostable timer keeping it active. If the pulses stop for a time greater than the time out period of the monostable timer 301, then the monostable timer 301 will time out and return to its stable state.

The operation of the missing pulse detector is illustrated in Figure 4 by showing the waveforms A, B and C at each stage. Thus, Figure 4 shows the high pass filter/differentiator 300 receiving a square wave pulse signal A and outputting, in response, a spiked signal B, each edge of which triggers the monostable timer 301. Whether or not the monostable timer 301 times out between successive spikes of the spiked signal B will, of course, depend upon the time out period of the monostable timer.

As will be explained in greater detail below, the controller 10 is arranged to interrupt the oscillator signal for a first time period when the data bit to be transmitted is a binary "0" and to interrupt the oscillator signal for a second different time period when the data bit to be transmitted is a binary "1". The fast missing pulse detector providing the first signal deriver 36 has a monostable timer 301 with a time out period so that this timer only times out and returns to its stable state when the oscillating signal supplied by the oscillator 21 is interrupted by the controller 10 for a period at least slightly longer than the oscillation period but well below the first time period (that is the time period for which the oscillator signal is interrupted when the data bit to be transmitted is a binary "0"). The pulse C output by the monostable timer 301 of the first signal deriver 36 will have one or two widths dependent on whether the particular data bit is a binary "0" or a binary "1".

The slow missing pulse detector providing the second signal deriver 36 has a monostable timer 301 with a time out period so that this timer only times out and returns to its stable state when the oscillating signal supplied by the oscillator 21 is interrupted by the controller 10 for a period having a duration in between the duration of the first and second periods where the second time period is the time period for which the oscillator signal is interrupted when the data bit to be transmitted is a binary "1". The pulse C output by the monostable timer 301 of the second signal deriver 36 will thus provide a pulse only when a particular data bit is a binary "1". As will be explained below, the control engine 33 determines from the state of the outputs of the fast and slow missing pulse derivers whether the received data bit is a 0 or 1.

Figure 5 shows one way in which the DTR circuitry 20 shown in Figure 2 may be implemented. In this embodiment, the oscillator 21 comprises a crystal oscillator X1 arranged to oscillate at an RF frequency of 13.56 megahertz (MHz) having one pin coupled to a ground power supply line 200 via a capacitor C12 and the other pin coupled to the ground power supply line via a capacitor C13. A resistor R5 is coupled across the crystal oscillator in parallel with a NAND gate ND1 whose output is coupled to the resistor R5 via a resistor R6. The other input of NAND gate ND1 is coupled to the power save output.

The oscillating signal is supplied from the output of the NAND gate ND1 to one input pin of a NAND gate ND2 which forms the gate 22. The other input of the NAND gate ND1 receives the gate signal from the controller 10.

The filter circuit 23 consists of a capacitor C5 coupled to the output of the NAND gate ND2 and coupled to the ground power supply line 200 via a capacitor C20 and via an inductor L3 to the inductor L1 of the tuned circuit part LC1. The junction between the inductors L3 and L1 is coupled to the ground power supply line via a capacitor C21. In this embodiment the capacitor C5 is a 10 nanofarad capacitor while the capacitors C20 and C21 are 180 picofarad capacitors and the inductor L3 is a 470 nanoHenry inductor.

The output of the tuned circuit part LC1 is supplied to the anode of an IN4148 diode D3 which forms the demodulator 24.

In this embodiment, the filter 25 consists of a resistor R1 and capacitor C6 coupled in parallel between the cathode of the diode D3 and the ground supply line and a resistor R2 and capacitor C7 coupled in series between the cathode of the diode D3 and the ground power supply line. The resistor R2 is coupled via a capacitor C8 to a first input of a first NAND gate ND3 of the buffer/squaring circuitry 26. The first input of NAND gate ND3 is also coupled via resistor R7 to the ground power supply line 200 and via series-connected resistors

R3 and R8 to its output. The junction J2 between resistors R3 and R8 is coupled via capacitor C11 to the ground supply line 200 while the output of the NAND gate ND3 is coupled via resistor R4 and capacitor C10 to the ground supply line 200 and via resistor R4 to the first input of a second NAND gate ND4. The second inputs of the NAND gates ND3 and ND4 are coupled to the power save line from the controller 10. The output of the NAND gate ND4 provides the demodulated, filtered, buffered and squared data signal to the data input of the controller 10.

Typical values for the components shown in Figure 5 whose values are not given above are shown on the drawing. It will, of course, be appreciated that the circuit shown in Figure 5 illustrates only one possible way of implementing the functional components of the DTR circuitry 20 shown in Figure 2.

Figure 6 shows a functional block diagram of the subsidiary unit illustrating in greater detail the components of the data storage device 30. The functional components of the subsidiary unit 4 are provided, in this example, on a printed circuit board (PCB). The data storage device 30 is provided as an integrated circuit (IC) to which the tuned circuit part LC2 is coupled. It may, however, be possible to provide an integrated circuit having all of the functional components of the subsidiary unit including the inductor L2.

As shown in Figure 6 one end of the tuned circuit part LC2 is coupled via the capacitor C3 to a modulation output pin MOD and via the capacitor C4 to an RF input pin RFIN1 while the other end of the tuned circuit part LC2 is coupled to a power supply pin Vss coupled to one of the two power supply lines 32 between which the diodes D1 and D2 are coupled. The power supply line 33 is coupled to a power supply pin Vdd which is coupled to Vss via a capacitor C30 provided externally of the IC and a resistor R30 provided on the IC. The IC also has a page select pin PS1 coupled to a page select input of the control engine 33 and a test pin TS coupled via a polycrystalline silicon fuse F to a test input of the control engine 33. The page select line L coupled between the page select pin PS1 and the control engine 33 is coupled to Vdd via a weak pull-up resistor R31. As will be described in detail below, the page select pin PS1 enables the control engine 33 to select one of a number (two in the embodiment to be described below) of pages of memory while the test pin TS enables complete memory erasure following testing.

As shown in Figure 6, the memory 23 consists of a hard wired memory area 230 which is defined by the metal layer mask during fabrication of the data storage device in known manner and a programmable non-volatile memory area 231 which consists, in this example, of electrically programmable and electrically erasable programmable ROM (EEPROM). The control engine 33 is coupled to the programmable memory 231 via data, address and page busses

DB, AB and PB. The non-programmable memory area 230 is coupled to the control engine 33 via a read bus RB to enable the ID to be read out and transmitted to the base module. The control engine 33 is also coupled to a charge pump 40 of conventional form that, in response to a signal from the control engine 33, generates (from the voltage Vdd) a voltage Vpp sufficient to enable altering of the state of a bit in the memory 231, that is writing to or erasing of the programmable memory 231. As illustrated schematically in Figure 6, a specific address or addresses A within the programmable memory 231 are allocated for storing a write-protect bit that enables the control engine 33 to determine whether or not writing to the programmable memory 231 is allowed. As another possibility, the write-protect bit may be provided as an independent bit on a page of the memory outside the normal addressable area of the memory 231.

In this embodiment, the non-programmable memory area 230 is capable of storing 16 bits and is arranged to store an identity code that is unique to the particular customer for the data storage device or to a type of data storage device. This identity code may be determined by the manufacturer of the device or may be determined in accordance with instructions received by the manufacturer from the customer for that specific device. Where the supply of the passive data storage device 30 or the data carried therein is licenced, then a portion of the non-programmable memory area may be defined by the licensor while the remaining bits may be available to the licensee

to distinguish between different products that might use the technology. For example, the first 12 bits may be defined by the licensor while the remaining 4 bits may be available to the licensee.

In this embodiment, the programmable memory 231 consists of two sections or pages and the control engine 33 is adapted to select the page of memory to be written to in dependence upon the state of the page select pin PS1. In this embodiment, the page select pin PS1 will only be accessible during manufacture of the passive data storage device 30 and accordingly writing of data to one of the two pages of the memory 231 will only be allowed during manufacture. This enables the memory 231 to contain an area of data that is protected from subsequent change or corruption by a user but which can be relatively easily changed or modified during manufacture.

Although not shown in Figure 6, the page select pin PS1 may, like the test pin TS, be coupled to the control engine 33 by a polycrystalline silicon fuse which is blown after the page has been written to to reduce the possibility of anybody being able to change or corrupt the data stored in that page by tampering with the packaging of the passive data storage device 30 so as to gain access to the page select pin PS1. In this embodiment, this page of the memory 231 consists of 8 bytes of memory while the remaining user-alterable page of the memory 231 consists of 64 bytes. For system reliability, part of the data space in each page of

memory is reserved for cyclic redundancy check (CRC) data.

As mentioned above, data is transmitted to the passive data storage device 30 by the controller 10 interrupting the carrier or oscillating signal provided by the oscillator 21.

Figure 7 shows schematically a signal I carrying data supplied to the tuned circuit part LC1 to illustrate how commands and/or data are transmitted to the passive data storage device by the base module 2 by interrupting the oscillating signal from the oscillator. The blocks B1 in Figure 7 represent bursts of the pulsed or oscillating 13.56 MHz carrier signal supplied by the oscillator 21 while short gaps G1 between blocks B1 represent digital zeros and long gaps G2 between blocks B1 represent digital ones. In this embodiment, the bursts B1 of the oscillator signal have a minimum duration of 40 μs and, typically, are 70 μs long. The short gaps or interrupts G1 representing digital zeros are 2 μs long while the long gap G2 representing digital ones are 16 μs long.

Figures 8a and 8b show the signals S1 and S2 input to the control engine 33 by the fast missing pulse detector 35 and the slow missing pulse detector 36, respectively, in response to receipt by the passive data storage device 30 of the signal I shown in Figure 7. As can be seen from Figures 7 and 8 and as discussed above, the fast missing pulse detector 35 provides a signal having a

pulse width (that is the period when the signal is low in Figures 8a and b)dependent on whether the received data bit is a binary zero (short pulse width W1) or a binary one (long pulse width W2). In contrast the slow missing pulse detector 36 provides a signal having pulses with a width W3 and a pulse is only produced when a data bit represents a binary one is received. The output from the fast missing pulse detector 35 is used by the control engine to derive its clock signal.

The response time of the slow missing pulse detector 36 is inherently longer than that of fast missing pulse detector 35 (generally the slow missing pulse detector will include a larger value capacitor)so that, as can be seen from Figures 8a and 8b, the rising edge of the pulse W2 produced by the fast missing pulse detector occurs a time t before the rising edge of the corresponding pulse W3. Thus, when the received data bit is a binary zero the rising edge of the pulse W1 occurs when the signal S2 is high while when the received data bit is a binary one the rising edge of the pulse W2 occurs when the signal S2 is low. The control engine 33 can thus determine whether a received data bit is a binary one or zero in dependence upon whether the outputs of the slow missing pulse detector 36 is high (binary zero) or low (binary one) at the rising edge of a pulse W1 or W2 of the fast missing pulse detector 35.

Figures 7 and 8 do not show the complete data transmission structure because, as will be explained in

greater detail below, in this embodiment the controller 10 is configured to cause each bit sent to be followed by an identical confirmation bit. Figure 9 shows the signal (001100) supplied to the control engine 33 by the first signal deriver 35 when the actual data transmitted is 010.

As will be described below, the control engine 33 is a state machine operable in a write, write-protect, test or read mode. In each case, when the control engine 33 receives data (either commands to be executed or data to be stored in the memory 231), it sets the state of its output OP in accordance with the state of the received data so that a signal corresponding to the received data is returned to the base module 2. Figure 10 which shows the output data signal supplied by the control engine 33 on its output OP corresponding to the input data signal shown in Figure 9 in modes other than the read mode. As can be seen from a comparison of Figures 9 and 10, on receipt of a data bit in modes other than the read mode, then, on the rising edge of the received signal, the control engine 33 outputs a return signal of the same logical state, that is 0 if the data bit is 0. However, when the confirmation bit is received, then, on the rising edge of the received signal, the control engine outputs as the return signal the inverse of the data. When the control engine is in the read mode it outputs the data bit read from memory followed by a confirmation bit which is the inverse of the read data bit. The advantage of inverting the return signal is that the

average of the signal received back by the base module should remain at the midpoint, regardless of the nature of the data.

The control engine 33 is adapted to enter the test mode when an erase command (or a command to fill the memory 231 with 1s or 0s to test the memory) is received while the test pin TS is held high and is adapted to enter the write mode or the write-protect mode in response to command signals from the base module. In this embodiment, the read mode is entered as a default mode if no command signal is received within a predetermined number of bits from power up, that is if sixteen zero bits are received in this example. The advantage of having the read mode as a default mode that is entered if no command is received is that the subsidiary unit may be used with a read only base module that expects a passive data storage device to transmit its data automatically without the need for a specific command.

Figure 11a shows diagrammatically the general structure of a command signal. A command signal consists of a start bit 50 for alerting the control engine 33 that a command code is to follow. The start bit is followed by an operation section 51 consisting of 4 bits (shown as xxxx in Figure 11a) that represent a code defining the particular type of command. For example, in this embodiment, the write command is "0011" while a write-protect command is "1010".

Figure 11b shows the signal structure provided by the base module 2 when writing to the passive data storage device 30. Thus, after the start bit (not shown in Figure 11b) and the write command 51a, the base module 2 waits for a short erase delay period 52 to give the passive data storage device 30 time to erase the page selected by the page select signal on pin PS1. The base module 2 then sends the data to be written into the selected page in sections 53 of N bits separated by delay periods 54. In this embodiment, each data section consists of n data bits plus one stop bit while the erase delay is 80 ms and the delay 54 between transmission of data sections is 10 ms. In this embodiment, the passive data storage device is arranged to disable itself once all the addresses in the selected page have been written to and the fact that the memory has entered a disabled state is indicated by the "disabled" section 55 in Figure 11b.

Figure 11c shows the structure of the write-protect command signal. As can be seen, this consists of a write-protect command 51b followed by a write-protect confirmation command 51c and then a short delay 56 (typically 10 ms) after which the passive data storage device 30 enters the disabled state.

Figure 11d shows a chip erase signal which, as explained above, is only effective when the test pin TS is held high. The chip erase signal consists of a chip erase command 51d followed by a short delay 57 (typically 10

ms) after which the passive data storage device 30 enters the disabled state. In this embodiment, the chip erase command is "1001".

As explained above, in this embodiment, the read mode is not activated by using a command having the structure shown in Figure 11a. Rather, the control engine 33 of the passive data storage device 30 is arranged to enter the read mode as the default mode if it receives a lead-in of zeros (sixteen in this embodiment), that is no command code is received.

Figure 12a shows the signal structure of the signal supplied by the control engine 33 in the read mode. Thus initially the control engine 33 returns the received data as described above without inversion. Accordingly, the signal structure includes a first return section 57 returning the 16 zero bit signal to the base module. This is followed by a header section 58, then first and second page sections 60 and 61 sending the page zero and the page 1 data respectively. The page 1 data is followed by a protect bit pattern 62 which confirms the status of the write-protect bit. In this embodiment, the protect bit pattern is a pattern of 8 bits with the pattern being "0xcc" when the page is write-protected and the pattern being "0xf0" when writing is permitted. The pattern is sent most significant bit first. Sending a protect bit pattern rather than the actual write-protect bit enables error detection.

Figure 12b shows the structure of the header section 58 of the read signal. As can be seen, this consists of a synchronisation pattern having a first section 58a consisting of 8 zero bits followed by a second section 58b consisting of a synchronisation bit. The synchronisation pattern provided by sections 58a and 58b enables the base module to synchronise itself with the incoming data stream to enable reading of the subsequent data. The synchronisation sections 58a and 58b are followed by a data section 58c consisting of the 16 bit ID read from the non-programmable memory area 230 and identifying the particular passive data storage device 30.

The operation of the data communication apparatus will now be described in greater detail with reference to the flow charts shown in Figures 13 to 22.

Figure 13 shows a flow chart for illustrating how the control engine 33 determines which state it should be in. Thus, assuming that the tuned circuit part LC2 of the subsidiary unit is coupled to the tuned circuit part LC1 of the base module 2 to form the tuned circuit, the control engine 33 is receiving an incoming signal at step S1 and the passive data storage device 30 is powered up, the control engine 33 determines at step S2 whether the signal includes a write, write-protect or erase command by checking any received command against a command look up table stored in its memory and, if a command is received, enters the appropriate mode. Where the

received command is the erase command, then the control engine 33 will not enter the erase mode unless the test pin TS is being held high. If no command is received then the control engine 33 defaults to the read mode at step S3.

Operation in the write mode will now be described with reference to Figure 14, 16 and 17.

Figure 14 shows a flow chart for illustrating the steps carried out by the controller 10 of the base module when writing is initiated. This is achieved by a user inputting instructions to the computer PC coupled to the base module 2 by the communications interface 8 to control operation of the controller 10.

When, at step S10 in Figure 14, the controller 10 receives from the computer instructions input by the user indicating that writing is to be initiated, then the controller 10 causes, via the communications interface 8, the computer PC to prompt the user to supply or identify the data to be written into the memory 230 of the passive data storage device 30 and stores that data in its memory 11 if it is not already present there. Then at step S12, the controller 10 sends the write command to the control engine 33 of the passive data storage device 30. At step S14, the control engine reads the first bit of data to be sent and checks at step S15 whether that data bit is a binary zero. If the answer is yes, then, at step S16, the controller 10 controls the

gate 22 to send the data bit zero and its confirmation bit by interrupting the carrier for a first time period to provide the gap G1, then allowing a burst B1 of the carrier signal, then interrupting the carrier again for the first time period and again allowing a burst B1 of the carrier signal. If, however, the answer at step S15 is no, then, at step S17, the controller 10 causes a data bit representing a binary 1 to be sent followed by its confirmation bit by interrupting the carrier signal for a second time period to provide the gap G2, then allowing a burst B1 of carrier signal, then interrupting the carrier signal again for the second time period and then allowing a burst B1 of the carrier signal.

The controller 10 then checks at step S18 whether all of the data bits have been sent and, if the answer is yes, the writing procedure ends. If, however, the answer at step S18 is no, then the controller 10 checks at step S20 whether N data bits have been sent and if so causes, after sending a stop bit, the delay 54 to occur (step S21). If, at step S22, an alarm signal is generated, indicating that writing is not occurring properly, then the controller 10 restarts the sending of the current set of N bits of data at step S23 and returns to step S15. If no alarm signal is generated, then the controller 10 reads the next data bit at step S24 and again returns to step S15.

The steps carried out by the passive data storage device 30 during the writing process will now be described with

reference to Figure 16 and 17 assuming that the passive data storage device 30 has already been powered up and has, as described with reference to Figure 13 above, received the write command causing the control engine 33 to enter the write mode.

Referring to Figure 16, the control engine 33 checks at step S30 whether the write-protect bit is set in the memory 231 and, if the answer is yes, disables writing to the memory at step S31 and sends a write-protected signal via its output OP to the base module 2 to enable the user to be advised that the memory 231 is write-protected. If the answer at step S30 is no, then the control engine 33 checks at step S32 if the page select signal PS1 is low. If the answer is yes, then the control engine 33 determines at step S33 that page 1 is selected. If, however, the answer is yes, then the control engine 33 determines at step S34 that page 0 is selected. At step S35, the control engine causes the selected page to be erased. Then at step S36, the control engine 33 receives the data transmitted by the base module 2 and stores it in the selected page of the memory 231.

Figure 17 shows step S36 of Figure 16 in greater detail. Thus, at step S360, the control engine 33 receives the signals from the slow and fast missing pulse detectors and determines as described above whether the received bit represents 1 or 0. At step S361 the control engine checks whether the received bit is the first of a pair

of received bits, that is whether the received bit is a data bit. If the answer is yes, then, at step S362, the control engine 33 stores the received data bit in its buffer 33a, sets its output OP to the same state as the data bit as described above with reference to Figures 9 and 10 and proceeds to step S365. If, however, the answer at step S361 is no, that is the received bit is a confirmation bit, then the control engine 33 sets its output to the inverse of the bit state as described above with reference to Figures 9 and 10 (step S363)and proceeds to step S364.

If the control engine 33 determines at step S364 that an alarm condition has occurred, then the control engine 33 causes its buffer 33a register to be cleared at step S364a and returns to step S360 awaiting the next bit. If, however, no alarm occurs, then the control engine 33 checks to see whether N data bits have been received at step S365 and if so stores those N data bits in the selected page of the memory 231 at step S366 then returns to step S360. If the answer at step S365 is no, then the control engine 33 returns to step S360 and awaits the next bit of data.

It will thus be seen from Figures 14, 16 and 17 that, during a writing process, data is supplied by the base module to the passive data storage device 30 in 8 bit sections with the delay between transmission of 8 bit sections enabling storage of the data in the selected page of the memory 231. If an alarm occurs, then the

control engine 33 clears its buffer 33a and the base module 2 commences rewriting of that N bit section or block of data into the memory 231. This enables rewriting of the data on the fly.

An alarm condition may be generated during the writing procedure at the base module if the controller does not receive back the data bits it expects (the data bit or the inverse of the confirmation bit) while an alarm condition may be generated at the passive data storage device if the data bit and confirmation bit do not agree. If an alarm condition occurs at the base module then the base module will as described above restart sending of the last N bit block of data while if an alarm condition is generated at the passive data storage device the passive data storage device will reset its buffer. Generation of an alarm at the passive data storage should automatically cause an alarm to be generated at the base module because the wrong data will be sent back.

Operation in the write-protect mode will now be described with reference to Figures 15a and 15b where Figure 15a shows the steps carried out by the base module and Figure 15b shows the steps carried out by the control engine 33 of the passive data storage device 30.

When at step S50 in Figure 15a the controller 10 of the base module determines that a user has instructed, via the personal computer PC coupled to the base module 2, that data stored in the memory 231 should be

write-protected, then the controller 10 sends the write-protect code (1010 in this embodiment). At step S52, the controller 10 checks on a bit-by-bit basis that the return signal from the passive data storage device is what it expects (that is the return of the data bit followed by the inverse of the confirmation bit), that is that the write-protect code is being correctly received. If not, an alarm is generated at step S55 and the procedure terminated. If, at step S52 in Figure 15a, the controller 10 of the base module determines that a correct returned write-protect code has been received, then the controller 10 checks, at step S53, whether the write-protect code has been sent twice and, if not, resends the write-protect code at step S56 and returns to step S52.

When at step S60 in Figure 15b the control engine 33 receives a write-protect code for the first time it enters the write protect-mode and checks at step S60a whether the write-protect code is being received for the second time. As this is not the case, then, at step S61, the control engine 33 controls its output to return the write-protect code to the base module 2 as described above with reference to Figures 9 and 10.

If an alarm condition occurs (that is a data bit does not agree with is confirmation bit)at step S62, then the control engine 33 enters a disabled state which prevents write-protection. Assuming that no alarm signal is received, then the control engine 33 then checks at step

S64 whether the write-protect command has been received twice and, if not, returns to step S60. When the write-protect code is being received for a second time, then the answer at step S60a is yes and the control engine proceeds to step S67 and returns the inverse of the write command as it is received. When the answer at step S64 is yes, that is the write-protect command has been received twice without error, then at step S65 the control engine 33 sets the write-protect bit of the memory 231. Setting of the write-protect bit is a permanent condition and cannot be reversed. Accordingly, after the write-protect bit has been set, the control engine 33 will cause the passive data storage device 30 to disable itself whenever any attempt is made to write to the passive data storage device 30. If at step S62 in Figure 15b an alarm code is received by the passive data storage device 30, then the control engine 33 immediately disables itself at step S63.

An alarm condition will arise at step S55 in Figure 15a if the controller 10 does not receive the correct write-protect command back from the control engine 10. Because the controller 10 is intentionally sending a write-protect command it expects the write protect command to be inverted by the passive data storage device when it is returned for the second time and so this does not generate an alarm at the base module. Inverting the write protect command on its second return provides protection against the passive data storage device accidentally being locked (write-protected)in the

extremely unlikely situation that, during a writing process, data being written into the passive data storage device inadvertently includes the write command. In this case because the controller 10 did not deliberately send the write-protect command it will not be expecting an inverted return signal and so an alarm will be generated on each return bit preventing accidental write-protecting. Similar considerations would apply if a passive data storage device is accidentally brought near a base module while it is write protecting another device because, in this case, that passive data storage device will not be in the write-protect mode and will not return the inverted write-protect command when expected by the controller 10.

As described above, the page of the memory 231 to which data is written is selected by the status of the page select pin PS1. The pin PS1 may be arranged so that after the passive data storage device 30 has been encapsulated and incorporated in the subsidiary unit 4, the pin PS1 cannot be accessed so that a user can only alter the content of one of the two pages of the memory 231. This means that the data stored in one of the two memory pages is available for modification by the end user while the other page of data is available for modification at the factory or manufacturing level but cannot be modified by the end user. This enables, for example, many passive data storage devices 30 each carrying the same metal layer option or ID or header to be manufactured and for the manufacturer to store

different data in different ones of the passive data storage devices. For example, where a set of subsidiary units with different characteristics are required, then the passive data storage devices for all subsidiary units may be manufactured so as to be identical with the only differences between the passive data storage devices being the data stored in the manufacturer-accessible page of the memory 231. As another possibility, the page select pin PS1 may be arranged so as to be accessible when the data storage device has been encapsulated in plastics material but not when the encapsulated data storage device is embedded within a subsidiary unit. This would enable the data storage devices to be manufactured independently from the subsidiary units and allow the manufacturer of the subsidiary units to store their own data in the manufacture accessible page of the memory.

Operation in the default read mode will now be described with reference to Figures 18 and 19 where Figure 18 shows steps carried out by the base module 2 while Figure 19 shows steps carried out by the passive data storage device 30.

The read mode may be activated by a user inputting instructions to a computer coupled to the communications port 8. The controller 10 of the base module 2 may, however, also be configured to cause the read mode command to be issued when the power on switch 7 is activated in the absence of any computer being coupled

to the communications port 8. This would enable the base module 2 to be used as a stand-alone read-only unit.

In either case, when the controller 10 determines at step S70 that reading is to be initiated, then at step S71 it sends the read "code" (in this case 16 zero bits) to the passive data storage device 30 of a subsidiary unit 4 placed on the subsidiary unit receiving area 3b.

When, at step S80 in Figure 19, the control engine 33 receives the a signal which does not contain a command (that is it receives the read "code"), then the control engine 33 enters the read mode by default and returns the read "code" (that is the received string of zeros) as it is received, as a lead-in. Then at step S81 in Figure 19, the control engine 33 reads the data stored in the non-programmable memory area 230, and outputs this as the header ID and then reads and sends the data in all of the pages (pages 0 and 1 in this case) followed by the write-protect bit pattern identifying the status of the write-protect bit and disables itself at step S82 indicating that it has sent all of its data.

The control engine 33 disables itself at step S82 until the passive data storage device 30 is powered down either by switching off of the base module 2 or removal of the subsidiary unit 4 from the vicinity of the subsidiary unit area 3b. As shown at step S73 in Figure 18, the base module 2 checks at step S73 whether it has correctly received the data from the passive data storage device

30. The data stored in the pages 0 and 1 of the memory include cyclic redundancy check (CRC) data or other error checking data that enables the controller 10 of the base module 2 to check the voracity of the received data in known manner.

If the controller 10 determines at step S73 that the data has been correctly received, then at step S74 the controller 10 stores the received data in its memory and at step S75 causes action to be executed in accordance with the received data. For example, if the received data incorporates an audio file, then the controller 10 may cause the loudspeaker 6 to issue sounds corresponding to that audio file. For example, where the subsidiary unit represents a figurine, then the audio file may contain speech characteristic of or identifying that figurine. As another possibility, where the figurine represents an animal, then the audio file may cause the loudspeaker 6 to issue a sound characteristic of that animal. The data downloaded from the passive data storage device 30 may also include data for causing messages to be displayed on the display 5 and/or data or instructions for supply by the communications interface 8 to the personal computer PC to, for example, cause messages to be displayed on the display screen of that personal computer or to affect or otherwise interact with a computer game or other piece of software being run by that computer.

If the answer at step S73 is no, then the controller 10 checks at step S76 whether a predetermined number x of attempts to read the data have been made and, if so, issues at step S77 an error message to the user (via the display 5, loudspeaker 6 or personal computer PC) and then terminates the reading attempt. If the answer at step S76 is no the controller 10 causes the subsidiary unit to power down at step S78 and then steps S71 to S73 are repeated.

In use of apparatus embodying the invention a user may re-programme the user programmable page of the memory 231 in the manner described above with reference to Figures 14 to 17 provided that the write-protect bit is not set. This may enable, for example, a user to generate their own audio files on a computer and to download these to a subsidiary unit 4. As another possibility, the data stored in the subsidiary unit 4 may be modifiable not directly by the user but as a result of actions taken by the user during the playing of a computer game on a computer or games console coupled to the base module 2.

As mentioned above, the passive data storage device 30 is provided with test pin TS and, when a high voltage is applied to this test pin, the control engine 33 enters a test mode. When the control engine 33 is in the test mode, then a user may send via a computer PC coupled to the communications interface 8 a chip erase command to cause the control engine 33 to erase the entirety of the memory 231 including the write-protect bit. This should

facilitate testing of the memory 231 by enabling a manufacturer, for example during development, to program the entirety of the memory 231 and to erase it at will. Figures 20 and 21 show the steps carried out by the base module 2 and passive data storage device, respectively, to effect erasure. Thus, at step S90 in Figure 20, when the controller 10 receives an erase command from a user, for example via a computer PC coupled to the base module 2 via the communications interface 8, the controller 10, at step S92, controls the gate 22 to interrupt the oscillator signal to supply the erase code to the passive data storage device. When, at step S93 in Figure 21, the control device 33 of the passive data storage device 30 receives the erase command while it is in the test mode (that is the test pen TS is held high), then at step S94 the control engine 33 causes the entirety of the memory 231, including the write-protect bit, to be erased at step S94. This enables the manufacturer or person responsible for storing the data in the non-user programmable page of the memory to erase the entirety of the memory and start again even if the write-protect bit has been set. After encapsulation of the passive data storage device, it is very difficult for anybody to access the test pin TS to enable erasing of the memory 231. However, it is possible that a determined person may be able to tamper with the packaging to access the test pin TS. Accordingly, the polycrystalline silicon fuse F is provided and is blown after the legitimate testing procedure has been completed and before encapsulation of the passive data storage device 30 so

as to prevent the possibility of an unauthorised person completely erasing and changing the content of the memory.

When the user programmable page of the memory 231 is not write-protected, then the content of that memory page can be changed by following the writing procedure discussed above. However, in this embodiment, a page of memory can only be updated or changed as a complete block so that, if it is desired to update only 1 byte, all 64 bytes have to be updated. Accordingly, when at step S11 in Figure 14 a user inputs to the base module 2 information indicating that part of the data to be stored in the memory 231 is already present in that memory, then the controller 10 first retrieves that data from the memory 231 by following the reading procedure described above and then modifies that data in accordance with any change required by the user before rewriting the data into the memory 231 following the steps set out above.

In the embodiment described above, during the writing procedure, individual N bit sections of data are buffered until the stop bit is received and the buffer is reset if an alarm is generated. Additionally or alternatively, confirmation that the data has been correctly stored in the memory may be effected by reading the data back from the memory 231 immediately it has been stored in the memory. This may be effected manually by the user or may be carried out automatically by the controller 10 being configured to cause a read command to be sent to the

passive data storage device 30 immediately after the writing process described above has been completed. In this case, if the data read back from the memory 231 is not correct, then the controller 10 may cause the memory 231 to be erased and the writing procedure to be repeated.

Typically, the time taken to write data into the memory 231 will, in the above described embodiment, be in the region of 800 milliseconds. It is possible that the subsidiary unit 4 may be removed (accidentally or deliberately) from the subsidiary unit receiving area 3b whilst the writing process is actually in progress. In these circumstances, the cyclic redundancy check should pick up any errors in the writing procedure and the controller 10 should be configured to alert the user (for example via a message displayed on the display 5 or output via the loudspeaker 6) that the writing process has failed because the subsidiary unit 4 was moved from the subsidiary unit receiving area 3b during the writing process. As a further back-up, the memory 11 of the base module 2 may contain a set of "default" data so that, if a subsidiary unit 4 freshly received on the subsidiary unit area 3b has corrupted data in its user programmable memory page, then the base module can automatically write the default data to that page to repair the passive data storage device. This procedure would, of course, not apply to the non-user programmable page of the memory 231.

Figure 22 shows a functional block diagram similar to Figure 2 of a modified version of the base module 2'. This version differs from that shown in Figure 2 in that the output of the buffer/squaring circuitry 26 is supplied directly to the non-inverting input of a comparator 260 and via an averaging circuit 261 to the inverting input of the comparator 260. The averaging circuit 261 will generally consist of an averaging capacitor connected between the inverting or negative input of the comparator 260 and ground by a transistor switch or transmission gate which is conducting while the carrier signal is present and after transients have settled but is off while the carrier is off and during carrier turn-on transients so that averaging is only carried out while there is a steady carrier signal. Switching of the transistor switch or transmission gate is achieved by control from the controller 10. As will be understood by those skilled in the art, the comparator 260 provides a high or low signal to the data input D, depending on whether the received data signal is above or below the average. This modification should facilitate determination by the controller 10 as to whether the received data signal represents a one or a zero. Generally, however, the introduction of the averaging circuitry 261 and accompanying comparator should not be necessary because the average of the signal will not vary much because the duration of the bursts B1 of carrier signal between the carrier interruptions determining the data signal will be significantly longer than the interruptions.

In the above described embodiments, data is output from the passive data storage device by the control engine 33 modulating, via the FET M1, the load on the inductor L1 of the tuned circuit part LC1. Other methods of modulating the carrier signal with the data read from the memory 23 may be used. Figure 23 shows a block diagram of another example of a base module 2" embodying the invention. This base module differs from that shown in Figures 2 and 22 in that phase modulation rather than amplitude modulation is used to transmit data from the passive data storage device 30 to the base module or reader 2. In this embodiment, the resonant frequency of the tuned circuit formed by the first and second tuned circuit parts LC1 and LC2 is slightly different from the carrier frequency so that the tuned circuit will oscillate at the frequency of the carrier signal with a phase offset from that of the carrier signal. In this embodiment, the output of the tuned circuit is supplied by a signal processor 40 to a phase detector 41.

The phase detector 41 receives the output of the signal processor 40 and also a phase reference signal from a phase reference circuit 43 coupled to the oscillator 21. The phase detector 41 compares the phase of the signal output by the signal processor 40 with the phase of the signal supplied by the phase reference 43 and supplies this to the positive input of a comparator 42a of comparing and averaging circuitry 42. The output of the phase detector 41 is also supplied to an averaging circuit 42b coupled to the negative or inverting input

of the comparator 42a which provides the data signal to the controller 10.

In operation of data communication apparatus using the base module shown in Figure 23, the switching on and off of the FET M1 in accordance with the data output signal on the output OP from the control engine 33 effectively switches the capacitor C3 into and out of the tuned circuit. The tuned circuit part LC2 and capacitor C3 are arranged such that the resonant frequency of the tuned circuit LC1 and LC2 when the capacitor C3 is coupled across the capacitor C2 is slightly below the frequency of the carrier signal and accordingly the tuned circuit will oscillate at the frequency of the carrier signal with a phase lag relative to that of the carrier signal. In contrast, when the capacitor C3 is not coupled into the tuned circuit part LC2, then the resonant frequency of the tuned circuit LC1 and LC2 is slightly greater than the frequency of the carrier signal and accordingly the tuned circuit will oscillate at the frequency of the carrier signal with a phase advance relative to that of the carrier signal.

The comparison and averaging circuitry 42 provides the controller 10 a signal which represents either a binary one or a binary zero, depending on whether the phase was advanced or retarded.

Although in the above described embodiment, the resonant frequency of the tuned circuit is different from that of

the carrier signal both when the capacitor C3 as coupled in parallel across the capacitor C2 and when it is not, it will be appreciated that one of these two frequencies may be the same as the carrier signal frequency provided by the oscillator. In another embodiment, neither of the two tuned circuit parts may actually be tuned to the carrier frequency.

Figure 24 shows an example of one way of implementing the data transmitting and receiving (DTR) circuitry 20a of the base module 2" shown in Figure 23. It will, however, be appreciated that Figure 24 shows only one way of implementing this circuitry and that there may be many different ways of implementing this circuitry. In view of this and because the contents of the circuit diagram shown in Figure 24 are self-explanatory, in the interests of simplicity, Figure 24 will not be described in detail herein.

Where the circuit shown in the circuit diagram of Figure 5 is implemented for the base module, then the capacitor C6 should be sufficient to avoid any switching transients resulting from the gating of the oscillating signal causing problems with the operation of the base module, in particular causing the signal average to vary which may cause the controller 10 difficulties in determining whether a data bit represents a 1 or a 0. It is possible to provide a capacitor C6 of sufficiently high value that the signal is sufficiently smoothed that the gap resulting from gating of the oscillator signal is jumped.

However, this would increase the settling time and so slow down the rate at which data can be transmitted.

Figure 25 shows a modified version of the circuit diagram shown in Figure 5. The circuit diagram shown in Figure 25 differs from that shown in Figure 5 in that an npn transistor T_A is coupled in series with the resistor R1 with the emitter of the transistor being coupled to the ground or zero volt line 200. The base of the transistor T_A is coupled to the gate line from the controller gate output GP via a resistor R_A. The transistor T_A is arranged to be rendered non-conducting when the gate signal goes low to interrupt the oscillating signal, so preventing switching transients causing pull-down of the voltage at the resistor R_1 when the gate is activated.

In the above described embodiments, communication between the passive data storage device and the base module is effected by inductive coupling to form a tuned circuit. It will be appreciated that the inductive coupling will not necessarily be by way of a tuned circuit. Also, other forms of coupling may be used. For example, the subsidiary unit 4 and subsidiary unit receiving area 3b may be configured so that placing the subsidiary unit 4 on the subsidiary unit receiving area 3b provides a direct ohmic coupling between the subsidiary unit and the base module.

Figure 26 shows a diagrammatic perspective view similar to Figure 1 of another example of data communication

apparatus embodying the invention while Figures 27 and 28 shows functional block diagrams of the base module and subsidiary unit shown in Figure 26. This data communication apparatus differs from that shown in Figures 1 to 3 in the way in which coupling is activated between the base module 2 and subsidiary unit 4. Thus, in this example, the tuned circuit parts LC1 and LC2 are replaced by sensing pads PC2 and PD1. One subsidiary unit 4 is shown in cross-section Figure 1. The subsidiary unit has an electrically conductive hollow body or casing 4'. A passive storage device 30 is mounted on an electrically insulating base 46 of the subsidiary unit. The sensing pad PD1 is provided as a copper layer on the exterior surface of the insulating base 46. Connection from the sensing pad PD1 to a signal line 42 (see Figure 3) of the data storage device 30 is provided via a plated hole 47 through the insulating layer 46 and a wire bond 48. A spring biassing member or clip 49, for example a beryllium wire, electrically connects a component of the passive data storage device to the conductive casing 4'.

It will, of course, be appreciated that the subsidiary unit 4 may have any shape desired or appropriate for the use required. The casing 4' may be cast from metal or may be moulded from an electrically conductive polymer, for example.

As shown by phantom schematic outlines in Figure 1, sensing pad PD2 is provided in the playing piece receiving area 3b in the form of an electrically

conductive area. The sensing pad PD2 is hidden beneath a paper or plastics top surface 3'a of the playing surface 3a and is thus shown in phantom lines.

The sensing pad PD2 is electrically coupled to a pcb (not shown) carrying functional components of the base or games module 2 via a conductive track and an appropriate pcb connector (not shown).

The sensing pad PD2 and conductive track are printed onto the underside of the top surface 3'a of the game board 3 by conventional printing techniques, such as screen printing of an electrically conductive material, typically a silver or carbon loaded conductive ink.

The sensing pad PD2 is adapted to couple capacitively to the sensing pad PD1 carried by the subsidiary unit 4 such that, when a user touches the casing 4', an electrical path is completed by the user back to the base module 2 to enable, as will be described in greater detail below, the passive data storage device carried by the subsidiary unit 4 to derive a power supply from a signal provided by the base module and to enable communication of data between the base module 2 and the subsidiary unit 4. Because only a capacitive coupling to the user is required the subsidiary unit may have a thin coating of paint or like material.

Typically the data storage device will require a 10μ (micro amp), 2.5 volt power supply.

Typically, the area of the sensing pads PD1 and PD2 may be in the range of from about 25mm² to more than 1000mm² depending on the power output of the oscillator 250. The sensing pad PD1 may be larger than the sensing pad PD2 and may for example occupy practically the entire area of the associated receiving area 3b so that precise location of a subsidiary unit is not required. Of course, the sensing pads PD1 and PD2 may have any desired footprint and need not be rectangular or square.

As can be seen from a comparison between Figures 2 and 27, the base module 2 shown in Figure 27 differs from that shown in Figure 2 in that the impedance Z is coupled to the sensing pad PD2 rather than to the tuned circuit part LC1.

Figure 28 shows a simplified block diagram of the functional components of the subsidiary unit. As can be seen from a comparison with Figure 3, this subsidiary unit differs from that shown in Figure 3 simply by virtue of the fact that the sensing pad PD1 (rather than the tuned circuit part LC2) is coupled to the junction J1. In this case, the diodes D1 and D2 thus derive a power supply for the passive data storage device 30 from the oscillating signal coupled to the passive data storage device when the sensing pads PD1 and PD2 are capacitively coupled and a user is in contact with the casing to complete an electrical path back to the base module via the casing 4'.

In this example, the oscillator is generally a 13.56 MegaHertz (MHz) oscillator. As described above, the gate 22 is coupled to a gate signal output port GP of the controller 10 so that the controller 10 can control whether or not a signal from the oscillator is supplied via the gate 22. The oscillator 21, gate 22, filter circuit 23, impedance Z and sensing pad PD2 provide, in operation, an oscillating signal which is supplied by the capacitive coupling between the sensing pads PD1 and PD2 to the passive data storage device carried by the subsidiary unit 4 when the subsidiary unit 4 is placed on the receiving area 3b and a user touches the casing 4' of the subsidiary unit to complete the return electrical path to the base module. A ground plane GRP may be provided to facilitate completion of the return path. As in the above examples, this oscillating signal provides a power supply for the passive data storage device 30 and interruption of the oscillator signal by a gate signal (GATE) supplied by the control engine 10 enables data transmission to the passive data storage device 30.

As will be appreciated from the above, there is only one electrically conductive track from the sensing pad PD1 to the base module 2. To enable power to be derived from the oscillator 21 signal, an electrical circuit must, of course, be completed.

In the embodiment described above, the only strong signal coupling between the games module 2 and a subsidiary unit

4 is between the two sensing pads PD1 and PD2. A ground (return) path is however provided via several means in differing proportions, depending upon the actual structure of the embodiment and the environment in which the apparatus is located. Examples of how the ground (return) path may be provided are shown in Figures 6a to 6e of WO 00/31676 the whole contents of which are hereby incorporated by reference and the applicants co-pending PCT application number: GB 01/03303 which claims priority from UK Application Number: 0018486.1.

The return path(s) that will be most significant in practice will depend upon the actual structure of the apparatus and environment. It will be appreciated that many of these return paths may occur via one or more man made or naturally occurring objects in the vicinity of the gaming apparatus and that, for example, whether or not an integrated ground plane GRP is necessary will depend on the electrical structure of the apparatus, for example the integrated ground plane may not be necessary if the apparatus is mains powered.

Reliance on the above types of return path is however, not necessary. Thus, an additional sensing area having an electrically conductive pad which makes direct ohmic contact to the negative terminal of the base module power supply may be provided so that the electrical circuit is completed when a user places his subsidiary unit 4 on the receiving area 3b and, while still in contact with the

subsidiary unit 4, touches the additional pad 3e as illustrated in Figure 6f or 6g of WO 00/31676.

As in the embodiment described with reference to Figures 1 to 3, a clock signal for the control engine 33 is derived from the oscillating signal supplied by the base module via a first signal deriver 35 coupled to the junction J1. The control engine 33 extracts data carried by the oscillating signal by using the output of the first signal deriver 35 and the output of a second similar signal deriver 36 coupled to the junction J1. A data output of the control engine 33 is coupled to a control gate of the FET M1 having one t_1 of its source and drain electrodes coupled via line 49 to the body or casing of the playing piece and via an impedance Z_M to the Vss power supply line 32. A shown the electrode t_1 is also coupled via a resistor R_M to the Vdd power supply 31, although this resistor may be omitted if there is a voltage clamp on the power supply. The other t_2 of the source and drain electrodes of the FET M1 is connected directly to the Vss power supply line 32. As will be described below, when data is output by the control engine 33 on the output line OP, the data switches the FET M1 on and off in accordance with the data. Switching on the IGFET T short circuits the impedance Z_M in series with the power supply to the data storage device 30, resulting in a varying load on the sensing pad PD1 which amplitude modulates the carrier signal in accordance with the data read out from the memory 23.

The oscillator impedance must, of course, be sufficient to enable the data storage device 30 to modulate the carrier signal and will typically be in the region of 500 ohms.

Figure 29 shows a functional block diagram of the subsidiary unit illustrating in greater detail the components of the data storage device 30. This differs from that shown in Figure 6 in the replacement of the tuned circuit part LC2 by the sensing pad PD1 and by the coupling between the sensing pad PD1 and the rest of the subsidiary unit. Thus, as can be seen from Figure 29 in this case, the sensing pad PD1 is coupled via the output pin RFINI to the anode of the diode D1, the main current path of the FET M1 is coupled between an output pin OD coupled via the clip 49 to the casing 4' (see Figure 26) and the power supply pin Vss. In addition, as mentioned above the impedance Zm is coupled between the main electrode of the FET M1 (that is between the pins MOD and Vss) and is coupled in series with the resistor Rm itself coupled between the pin MOD and the power supply pin Vdd. Of course, the values of the components in this circuit may differ from those shown in Figure 6.

As in the above described embodiments, the data output by the control engine 33 is extracted from the modulated oscillating signal by the demodulator 24, the filter 25 and buffer/squaring circuitry 26 to provide a data input signal to the controller 10 (Figure 27). Also, the process of writing to the subsidiary unit is the same as

described above, the only difference being the manner in which coupling between the base module and subsidiary unit is achieved.

As shown in Figure 30, the modification illustrated in Figure 22 of the base module shown in Figure 2 may be applied to the base module shown in Figure 27.

In the embodiments described with reference to Figures 26 to 30, data is output from the passive data storage device by the amplitude modulation. Other methods of modulating the carrier signal with the data read from the memory 23 may be used such as phase modulation as described in WO 97/23060 or frequency modulation. Also the sensing pads PD1 and PD2 are capacitively coupled. However, other forms of coupling may be used. For example, the subsidiary unit 4 and subsidiary unit receiving area 3b may be configured so that placing the subsidiary unit 4 on the subsidiary unit receiving area 3b provides a direct ohmic coupling between the sensing pads of the subsidiary unit and the base module. In addition, the passive data storage device described with reference to Figures 26 to 30 is based on that shown in Figure 4 of the above-mentioned co-pending PCT Application Number: GB 01/03303 modified to incorporate the clock pulse deriver 35 and data deriver 36. The passive data storage device may however be based on the passive data storage device shown in Figure 4 of WO 00/31676. Also, as described above, a single subsidiary unit receiving area is provided. However, many such

receiving areas may be provided and the apparatus may have the structure described in WO 00/31676 with respect to Figures 1, 2 and 3 thereof, for example, with the base module being arranged to address each sensing pad PD2 in turn.

In the above described embodiments, data and/or commands are communicated to the passive data storage device from the base module by interrupting the carrier signal with short and long interruptions representing digital zero and one, respectively. It will, of course, be appreciated that these could be reversed and that different ways of communicating data and/or commands (for example amplitude, phase or frequency modulation) may be used.

In the above described embodiments, the same base module 2 is used to write data into the non-user programmable page and the user programmable page of the memory 231. It will, however, be appreciated, that, in practice, writing of data into the non-user programmable page or area of the memory 231 may be effected using a separate dedicated device.

In the above described embodiments, the base module 2 is coupled to a computer to facilitate writing of data into the base module. The base module itself may, however, be arranged to couple directly to a user input device such as a keyboard or may be arranged to download data from a removable disc received in a removable disc drive

coupled directly to the controller 10 rather than via a computer system. The communications interface 8 may also be arranged to couple to a network to enable data and/or command to be downloaded as a signal over the network.

The present invention may be applied to toys and games and to educational games structures such as, for example, globes representing the earth or other bodies with, in this case, a subsidiary unit receiving area or areas being located at a specific geographical location such that when a user brings a subsidiary unit into contact with a sensing a subsidiary unit receiving area, information stored in its memory regarding that geographic location is presented to the user.

The present invention may be applied to gaming tables and the like.

The present invention may also have applications outside the toy, educational and gaming industries. For example, the present invention may have applications in the asset tracking or tagging field where the data storage device is associated with a document or product, in which case the permanent ID stored in the hard-wired memory area 230 and/or the data stored in the non-user programmable memory page may be security information for tracking the document or product.

In the above described embodiments, the base module has a single subsidiary unit receiving area. The base module

may, however, have a plurality of subsidiary unit receiving areas each having their own tuned circuit part or coupler and the coupler may be connected by a multiplexer to the oscillator or to the demodulator or may be connected by respective individual DTR circuitry to a multiplexer connected to the controller 10.

Also, the memory may have a different configuration to that described above. For example the programmable memory may have many more pages and the non-programmable memory area 230 may be larger, in which case it would generally be formed of Mask ROM. Also, different types of programmable memory may be provided, for example a non-volatile programmable memory may be used such as, for example, flash memory. In addition at least part of the memory may be one time programmable (OTP) which would not need write-protection facilities. Also, at least part of the programmable memory may be volatile memory such as RAM (possibly with capacitor power storage to increase the data retention time) which stores data for only a short period of time. Also it may be possible to write-protect only a single page of the memory. In addition, the control engine 33 may store a look up table (LUT) that contains data giving the characteristics of each part of memory so that the control engine determines from this LUT whether a section of memory can be written to, is read only, or is write-protected. In this case all of the memory could be programmable and the control engine 33 would determine whether or not a user may program a particular section of memory section of memory.

Also, page selection need not necessarily be by way of a page selection signal but may be by way of a command from the base module.

The subsidiary unit may be coupled to a transducer such as a temperature, humidity or pressure sensor. In this case the base module will be arranged to cause the control engine 33 to read the status of the transducer when the passive data storage device is powered up and to cause the read data to be transmitted to the base module which may then cause the passive data storage device to enter the write mode to enable the time, date and value of the transducer reading to be stored in the programmable memory 231.

In one aspect, the present invention provides a data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having signal supplying means for supplying a signal to the subsidiary unit when the first and second electrical coupling means are coupled and data communicating means for interrupting the signal in accordance with data to be communicated to the subsidiary unit to provide to the first coupling means an interrupted signal having interruptions dependent upon

the data to be communicated, and the subsidiary unit having data extracting means for extracting the data from an interrupted signal supplied to the subsidiary unit and data storing means for causing the extracted data to be written into the memory.

In one aspect, the present invention provides a data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having data signal supplying means for supplying a data signal to the subsidiary unit when the first and second electrical coupling means are coupled, the subsidiary unit having data receiving means for receiving a data signal, data buffering means for buffering received data until a predetermined amount of data has been received and data storing means for causing the buffered data to be written into the memory when the predetermined amount has been received.

In one aspect, the present invention provides a data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first

electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having data signal supplying means for supplying a data signal to the subsidiary unit when the first and second electrical coupling means are coupled, the subsidiary unit having data receiving means for receiving a data signal, data buffering means for buffering received data until a predetermined amount of data has been received, checking means for checking whether data is received correctly, resetting means for erasing the contents of the data buffering means when data is not received correctly and data storing means for causing the buffered data to be written into the memory when data is received correctly.

In one aspect, the present invention provides a data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having data signal supplying means for supplying data in blocks to the subsidiary unit when the first and second electrical coupling means are coupled, and the subsidiary unit having data receiving means for receiving blocks of data, data buffering means for buffering the data until a block of data has been received, data returning means for returning the data back to the base

module as the data is received, and data storing means for causing the buffered data to be written into the memory when a block of data has been received, the base module also having data receiving means for receiving data from the subsidiary unit, data comparing means for comparing data returned by the subsidiary unit with the data supplied by the data signal supplying means, and control means for causing the data signal supplying means to resend the last block of data again to the subsidiary unit when the returned data does not agree with the data supplied by the data signal supplying means.

In one aspect, the present invention provides a data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having signal supplying means for supplying a data signal to the subsidiary unit when the first and second electrical coupling means are coupled, the subsidiary unit having data receiving means for receiving a data signal, and data storing means for causing the received data to be written into the memory, wherein the memory of the subsidiary unit has at least two memory areas and the subsidiary unit has memory area selecting means for selecting the area of the memory in which the data

storing means is to store data by the data receiving means.

In one aspect, the present invention provides a data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having signal supplying means for supplying a data signal to the subsidiary unit when the first and second electrical coupling means are coupled, the subsidiary unit having data receiving means for receiving a data signal, and data storing means for causing the received data to be written into the memory, the memory having a memory region into which data can be written by the data storing means and a memory region that is preconfigured during manufacture and cannot be programmed.

In one aspect, the present invention provides a data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having data signal supplying means for supplying

a data signal to the subsidiary unit when the first and second electrical coupling means are coupled, and the subsidiary unit having data receiving means for receiving the data and data storing means for causing the received data to be written into the memory, wherein the memory is arranged to have either a write-allowed or a write-protected status with an area of the memory being designated as a write protect area, the base module has control means for causing the data signal supplying means to supply write-protect data to the subsidiary unit, and the data storing means is arranged to cause received write-protect data to be stored in the write protect area so that the memory has the write-protected status, and the subsidiary unit has data storage prevention means for preventing writing of data into the memory when the write protect area stores data indicating that the memory is write-protected such that the write-protected status is irreversible.

In one aspect, the present invention provides a data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having data signal supplying means for supplying a data signal to the subsidiary unit when the first and second electrical coupling means are coupled, and the

subsidiary unit having data receiving means for receiving the data and data storing means for causing the received data to be written into the memory, wherein at least a part of the memory is arranged to have either a write allowed or a write protected status, the base module is arranged to provide a write protect instruction by sending a write protect command and the subsidiary unit is arranged to cause the write protect command to be at least partially inverted and returned to the base module, the subsidiary unit being arranged to cause at least part of the memory to be write protected when the write protect command is correctly received.

In one aspect, the present invention provides a data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having signal supplying means for supplying a signal to the subsidiary unit when the first and second electrical coupling means are coupled and data communicating means for interrupting the signal in accordance with data to be communicated to the subsidiary unit to provide to the first coupling means an interrupted signal having interruptions dependent upon the data to be communicated, the data communication means being arranged to send the data as data bits each

followed by a confirmation bit and the subsidiary unit having data returning means for modifying the received signal to return the received data as it is received so that each returned data bit is followed by the inverse of the corresponding confirmation bit.

In another aspect, there is provided a base module having the base module features set out in any one of the above aspects.

In another aspect, there is provided a subsidiary unit having the subsidiary unit features set out in any of the above aspects.

There is also provided a game or toy having data communication apparatus, a base module or a subsidiary unit in accordance with any one of the preceding aspects.

Throughout this specification and the claims which follow, unless the context requires otherwise, the word "comprise", or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated integer or group of integers but not the exclusion of any other integer or group of integers.

Other modifications will be apparent to those skilled in the art.

CLAIMS

1. A data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having signal supplying means for supplying a signal to the subsidiary unit when the first and second electrical coupling means are coupled and data communicating means for interrupting the signal in accordance with data to be communicated to the subsidiary unit to provide to the first coupling means an interrupted signal having interruptions dependent upon the data to be communicated, the data communication means being arranged to send the data as data bits each followed by a confirmation bit and the subsidiary unit having data returning means for modifying the received signal to return each received data bit as it is received so that each returned data bit is followed by the inverse of the corresponding confirmation bit.

2. Apparatus according to claim 1, wherein the data communicating means is arranged to interrupt the signal for a first time period when the data represents a binary zero and to interrupt the signal for a second time period when the data represents a binary one.

3. Apparatus according to claim 1, wherein the data communicating means is arranged to interrupt the signal for a first time period when the data represents a binary zero and to interrupt the signal for a second time period longer than the first time period when the data represents a binary one.

4. Apparatus according to any one of the preceding claims, wherein the signal supplying means is arranged to supply an oscillating or pulsed signal as the signal.

5. Apparatus according to claim 2 or 3, wherein the signal supplying means is arranged to supply an oscillating or pulsed signal as the signal and the subsidiary unit comprises missing pulse detectors for detecting the interruptions.

6. Apparatus according to claim 5, wherein the missing pulse detector comprises monostable timers adapted to time out in response to an interruption of the signal.

7. Apparatus according to any one of claims 4 to 6, wherein the subsidiary unit has clock signal generation means for generating a clock signal for the subsidiary unit from the oscillating or pulsed signal.

8. Apparatus according to claim 7, wherein the clock signal generation means comprises a missing pulse detector adapted to provide a clock signal from the oscillating or pulsed signal.

9. Apparatus according to claim 8, wherein the missing pulse detector comprises a monostable timer adapted to time out in accordance with the pulses or oscillations of the signal.

10. Apparatus according to claim 2 or 3, wherein the signal supplying means is arranged to supply an oscillating or pulsed signal as the signal, the subsidiary unit has clock signal generation means for generating a clock signal for the subsidiary unit from the oscillating or pulsed signal, the subsidiary unit comprising relatively slow and relatively fast missing pulse detectors for detecting the interruptions and the clock signal generation means comprises the relatively fast missing pulse detector.

11. Apparatus according to any one of the preceding claims, wherein the subsidiary unit has power supply deriving means for deriving a power supply for the subsidiary unit from the signal.

12. Apparatus according to any one of the preceding claims, wherein the signal supplying means is arranged to supply the signal via the first and second coupling means when the subsidiary unit is received by the subsidiary unit receiving area.

13. Apparatus according to any one of the preceding claims, wherein the base module has data receipt determining means for determining whether a returned

confirmation bit is the inverse of the corresponding returned data bit data and is arranged to generate an alarm if not.

14. Apparatus according to to any one of the preceding claims, wherein the subsidiary unit has erasing means for causing data to be erased when a confirmation bit does not agree with the corresponding data bit.

15. Apparatus according to claim 13, wherein the data communicating means is arranged to resend data when an alarm is generated.

16. Apparatus according to any one of the preceding claims, the subsidiary unit further comprising data buffering means for buffering received data until a predetermined amount of data has been received and data storing means for causing the buffered data to be written into the memory when the predetermined amount has been received.

17. Apparatus according to any one of the preceding claims, the subsidiary unit further comprising checking means for checking whether data is received correctly, resetting means for erasing the contents of the data buffering means when data is not received correctly and data storing means for causing the buffered data to be written into the memory when data is received correctly.

18. Apparatus according to any one of claims 1 to 15, wherein the data communicating means is arranged to communicate data in blocks to the subsidiary unit when the first and second electrical coupling means are coupled, and the subsidiary unit has data buffering means for buffering the data until a block of data has been received, and data storing means for causing the buffered data to be written into the memory when a block of data has been received, the base module also having data comparing means for comparing data returned by the subsidiary unit with the data supplied by the data communicating means, and control means for causing the data signal supplying means to resend the last block of data again to the subsidiary unit when the returned data does not agree with the data supplied by the data signal supplying means.

19. Apparatus according to claim 18, wherein the subsidiary unit has data checking means for checking whether data is received correctly and resetting means for erasing the contents of the data buffering means when data is not received correctly.

20. Apparatus according to any one of claims 1 to 17, wherein the data communicating means is arranged to communicate data in blocks and the base module has data receipt determining means for determining whether a returned confirmation bit is the inverse of the corresponding returned data bit data and alarm generating means for generating an alarm if not.

21. Apparatus according to claim 20, wherein the subsidiary unit has checking means for checking whether a confirmation bit agrees with its data bit and erasing means for causing the last block of data to be erased if not.

22. Apparatus according to claim 20 or 21, wherein the data communicating means is arranged to resend the last block of data when an alarm is generated.

23. Apparatus according to any one of the preceding claims, wherein the memory of the subsidiary unit has at least two memory areas and the subsidiary unit has memory area selecting means for selecting an area of the memory means to be used to store data.

24. Apparatus according to claim 23, wherein the memory area selecting means is preset and encapsulated so that, after encapsulation, data can only be written into one of said two memory areas.

25. A data communication apparatus, comprising:

a base module having a subsidiary unit receiving area having first electrical coupling means; and

a subsidiary unit having a memory and second electrical coupling means arranged to couple to the first electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area, the base module having signal supplying means for supplying a data signal to the subsidiary unit when the first and second

electrical coupling means are coupled, the subsidiary unit having data receiving means for receiving a data signal, and data storing means for causing the received data to be written into the memory, wherein the memory of the subsidiary unit has at least two memory areas and the subsidiary unit has memory area selecting means for selecting the area of the memory in which the data storing means is to store data by the data receiving means, wherein the memory area selecting means is preset and encapsulated so that, after encapsulation, data can only be written into one of said two memory areas.

26. Apparatus according to claim 25, wherein the data signal supplying means comprises signal supplying means for supplying a signal to the subsidiary unit when the first and second electrical coupling means are coupled and data communicating means for interrupting the signal in accordance with data to be communicated to the subsidiary unit to provide to the first coupling means an interrupted signal having interruptions dependent upon the data to be communicated, and the subsidiary unit signal receiving means has data extracting means for extracting the data from an interrupted signal supplied to the subsidiary unit.

27. Apparatus according to claim 23, 24 or 25, wherein the memory area selecting means comprises a memory area select input pin and memory area determining means for selecting the memory area in accordance with the status of the memory area select input pin.

28. Apparatus according to claim 27, wherein the subsidiary unit is provided within a housing and the select pin is arranged to be accessible only prior to the subsidiary unit being placed within the housing such that after the subsidiary unit has been placed in the housing data can be written into only one memory area.

29. Apparatus according to any one of the preceding claims, wherein the memory is arranged to have either a write-allowed or a write-protected status, an area of the memory is designated as a write protect area and the subsidiary unit has data storage prevention means for preventing writing of data into the memory when the write protect area stores data indicating that the memory is write-protected.

30. Apparatus according to claim 29, wherein the base module has control means for causing the data communicating means to communicate write-protect data to the subsidiary unit and the subsidiary unit is arranged to cause the write-protect data to be stored in a write protect area so that the memory has the write-protected status.

31. Apparatus according to claim 29 or 30, wherein the write-protected status is irreversible.

32. Apparatus according to claim 31, wherein the subsidiary unit has a test pin input that enables overriding of the write-protected status during testing

and a fusible link is fused after testing to prevent further overriding of the write-protected status.

33. Apparatus according to any one of the preceding claims, wherein the memory has a region that is preprogrammed and is not reprogrammable.

34. Apparatus according to claim 33, wherein the preprogrammed memory region is hard wired during manufacture.

35. Apparatus according to claim 34, wherein the content of the preprogrammed memory region is determined by a metal layer mask pattern during manufacture.

36. Apparatus according to any one of the preceding claims, wherein the first and second electrical coupling means are arranged to couple inductively.

37. Apparatus according to claim 36, wherein the first and second electrical coupling means comprise respective parts of a tuned circuit.

38. Apparatus according to any one of claims 1 to 35, wherein the first electrical coupling means are arranged to couple to the second electrical coupling means when the subsidiary unit is received on the subsidiary unit receiving area so as to complete an electrical path via a user back to the base module.

39. Apparatus according to claim 38, wherein said second electrical coupling means is arranged to couple to the user when the user makes contact with or is in close proximity to the subsidiary unit.

40. Apparatus according to claim 38 or 39, wherein the first and second electrical coupling means are arranged so as to couple capacitively to one another or so as to make a direct ohmic connection.

41. A base module having the base module features set out in any one of claims 1 to 40.

42. A subsidiary unit having the subsidiary unit features set out in any one of claims 1 to 40.

43. A base module having first electrical coupling means for coupling to second electrical coupling means of a subsidiary unit having a memory, the base module having signal supplying means for supplying a signal to the subsidiary unit when the first and second electrical coupling means are coupled and data communicating means for interrupting the signal in accordance with data to be communicated to the subsidiary unit to provide to the first coupling means an interrupted signal having interruptions dependent upon the data to be communicated, the data communicating means comprising control means and a logic gate controllable by the control means to control whether or not the signal supplied by the signal

supplying means is supplied to the first electrical coupling means.

44. A base module according to claim 43, wherein the logic gate is a NAND gate.

45. A base module according to claim 43 or 44, wherein an output of the logic gate is supplied to the first electrical coupling means by an LC filter.

46. A base module according to claim 43, 44 or 45, wherein the signal supplying means comprises a crystal oscillator circuit including a NAND gate.

47. A base module according to any one of claims 43 to 46, having data extracting means comprising a demodulator, filter and a buffer circuit.

48. A base module according to claim 47, having at least one of the following features:

the demodulator is a single diode;

the filter is an RC filter; and

the buffer circuit comprises a NAND gate circuit.

49. A base module according to any one of the preceding claims 43 to 48, consisting essentially of passive components and logic gates.

50. A base module according to any one of claims 43 to 49, having the base module features set out in any one of claims 1 to 40.

51. A games apparatus comprising a data communication apparatus in accordance with any one of claims 1 to 40, wherein the subsidiary unit is a playing piece.

52. A toy or game comprising a data communication apparatus in accordance with any one of claims 1 to 40 or a base module in accordance with any one of claims 43 to 50.

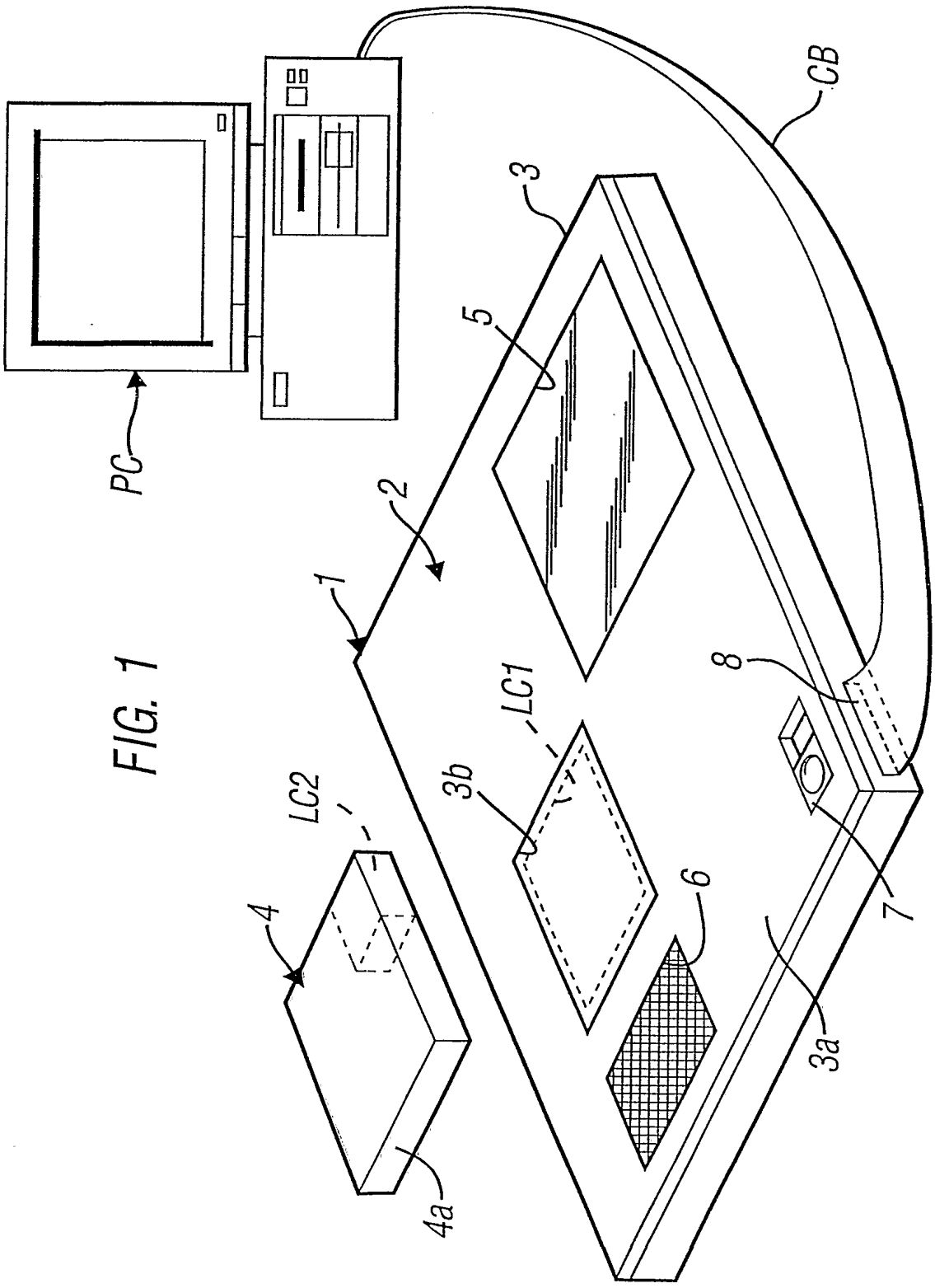


FIG. 1

FIG. 2

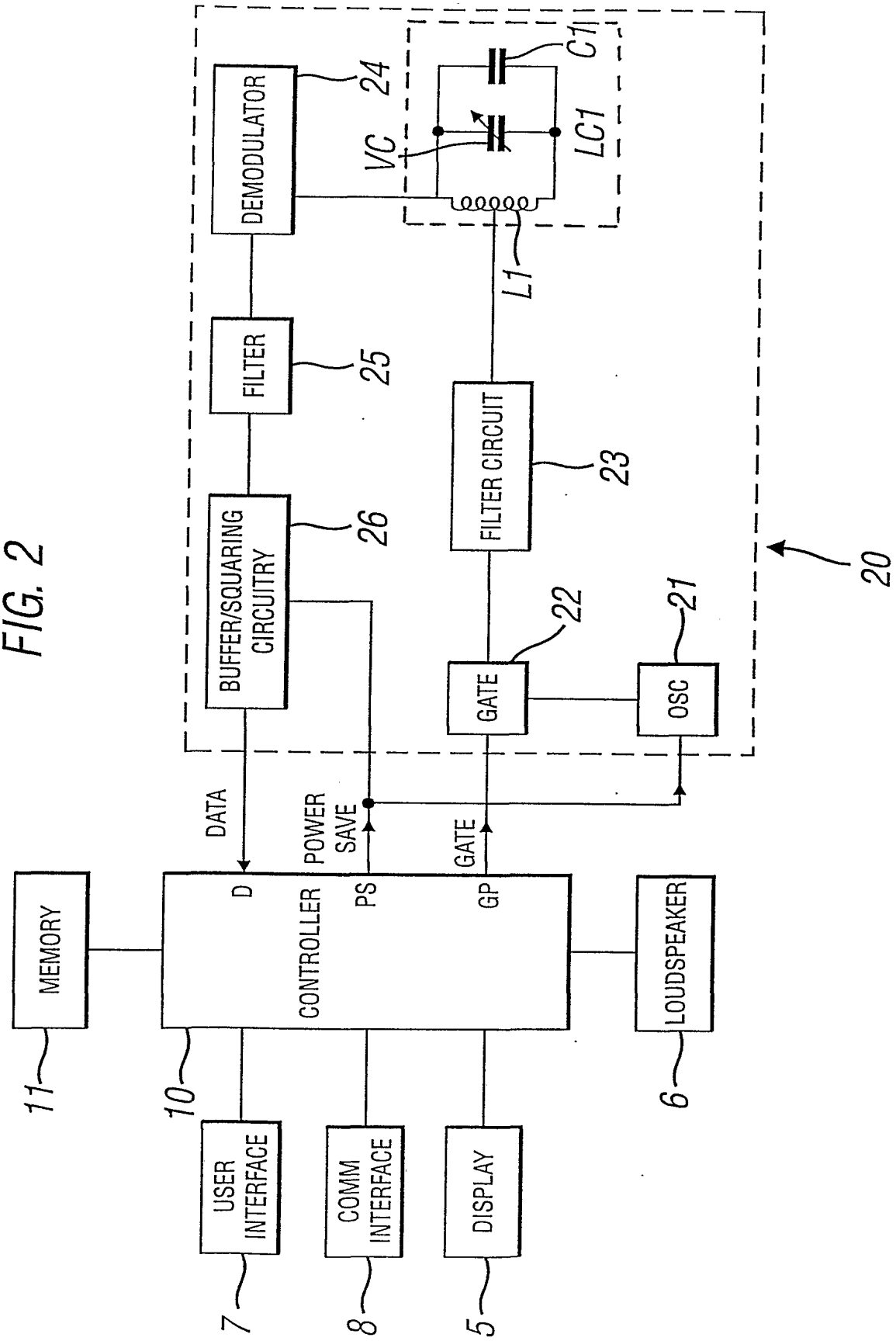

DEMODULATOR
24
VC
C1
LC1
L1
FILTER
25
FILTER CIRCUIT
23
BUFFER/SQUARING CIRCUITRY
26
GATE
22
OSC
21
20
DATA
POWER SAVE
GATE
D
PS
GP
CONTROLLER
MEMORY
LOUDSPEAKER
11
10
6
USER INTERFACE
COMM INTERFACE
DISPLAY
7
8
5

FIG. 3

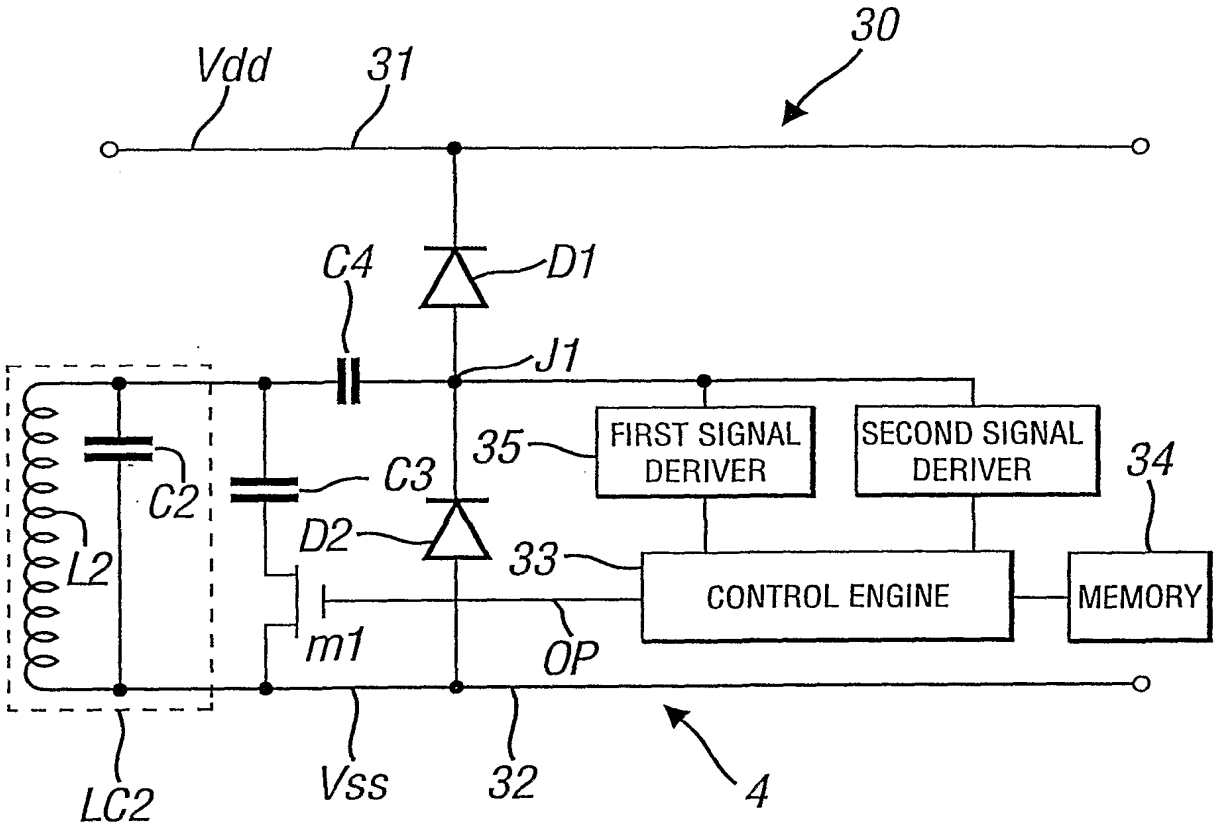

30
Vdd
31
C4
D1
J1
C2
C3
35
FIRST SIGNAL DERIVER
SECOND SIGNAL DERIVER
34
L2
D2
33
CONTROL ENGINE
MEMORY
m1
OP
LC2
Vss
32
4

FIG. 4

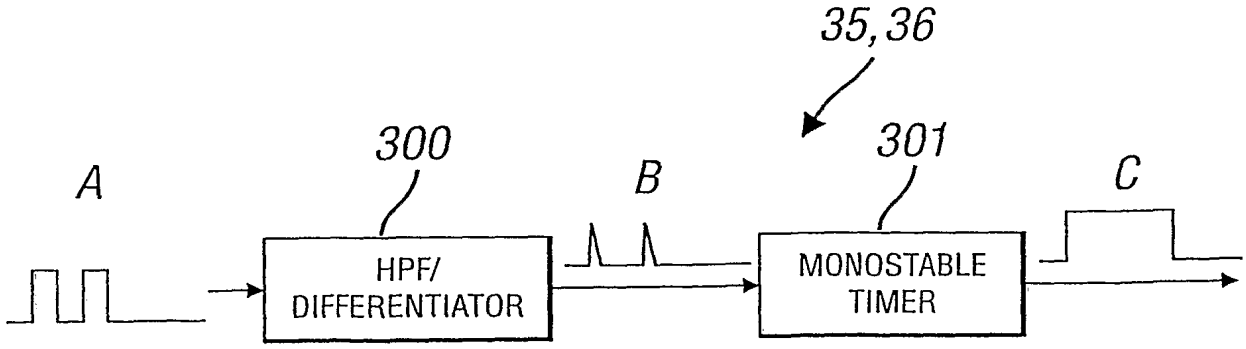

35,36
300
301
A
B
C
HPF/ DIFFERENTIATOR
MONOSTABLE TIMER

FIG. 5

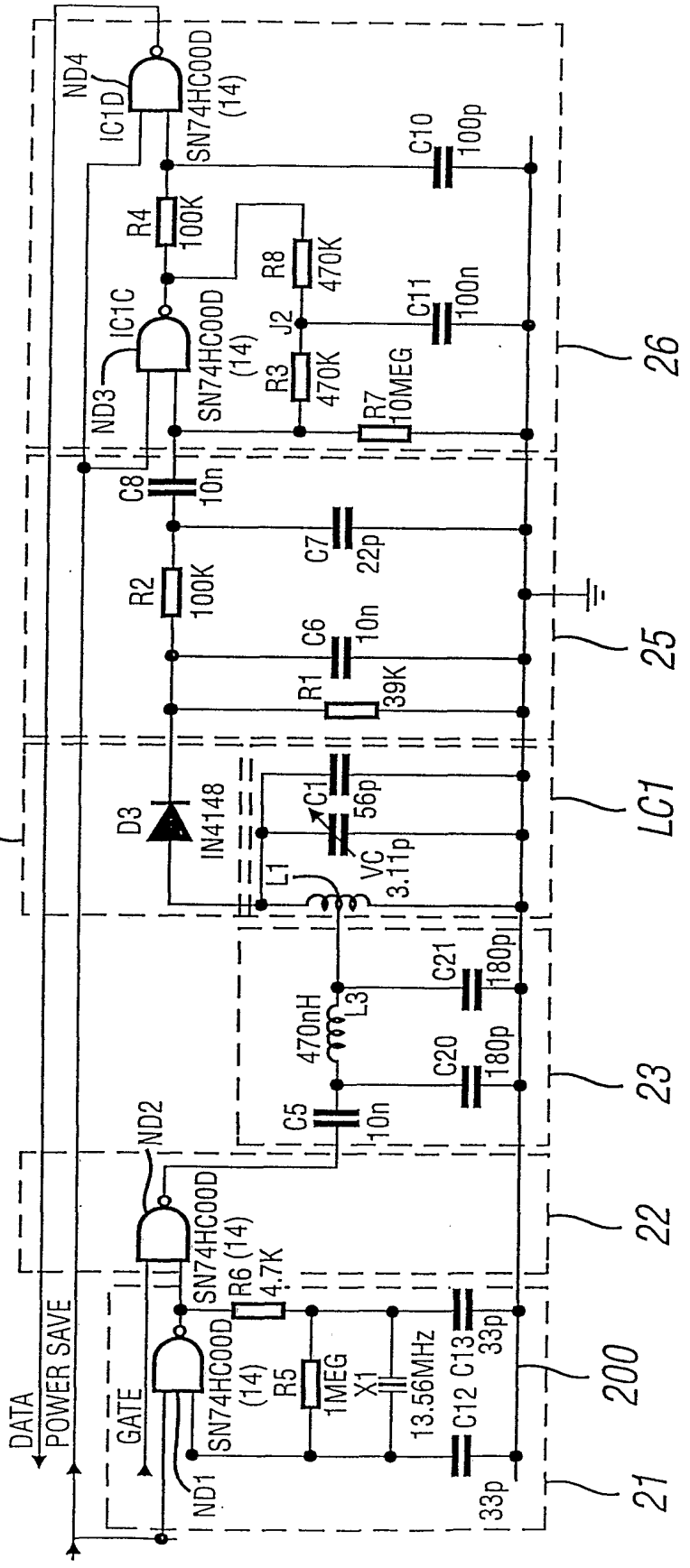

24
ND4
IC1D
SN74HC00D
(14)
C10
100p
R4
100K
R8
470K
IC1C
J2
C11
100n
ND3
SN74HC00D
(14)
R3
470K
R7
10MEG
26
C8
10n
C7
22p
R2
100K
C6
10n
25
R1
39K
D3
IN4148
C1
56p
VC
3.11p
L1
LC1
C21
180p
470nH
L3
C20
180p
C5
10n
23
ND2
SN74HC00D
(14)
R6
4.7K
22
DATA
POWER SAVE
GATE
SN74HC00D
(14)
R5
1MEG
X1
13.56MHz
C12
C13
33p
200
ND1
33p
21

FIG. 6

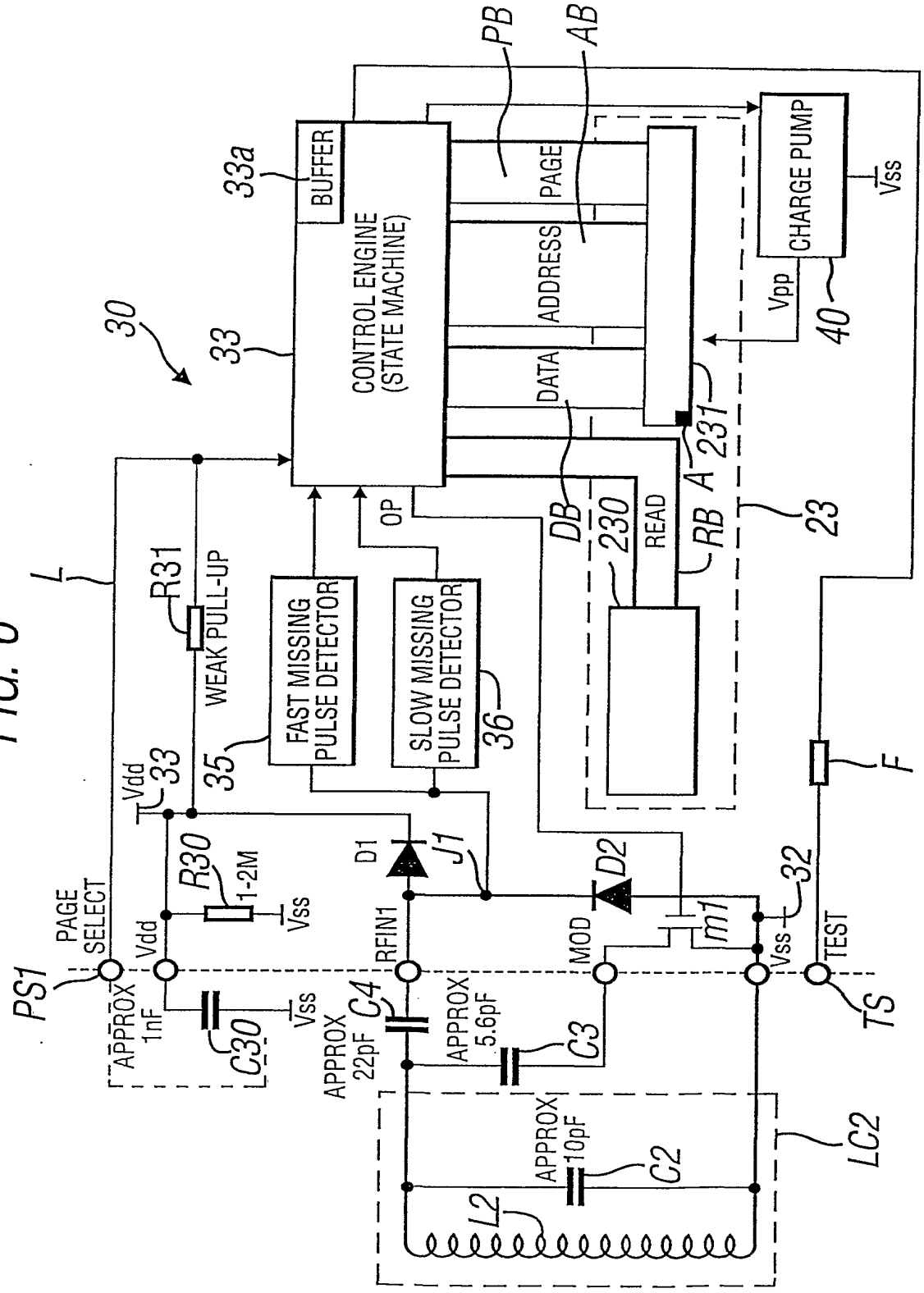

30
33
33a
BUFFER
CONTROL ENGINE (STATE MACHINE)
PB
AB
PAGE
ADDRESS
DATA
231
CHARGE PUMP
Vpp
40
Vss
DB
230
READ
RB
A
23
OP
L
R31
WEAK PULL-UP
FAST MISSING PULSE DETECTOR
35
SLOW MISSING PULSE DETECTOR
36
F
Vdd
33
R30
1-2M
Vss
D1
J1
D2
m1
32
PAGE SELECT
PS1
Vdd
RFIN1
MOD
Vss
TEST
TS
APPROX 1nF
C30
APPROX 22pF
C4
APPROX 5.6pF
C3
APPROX 10pF
C2
L2
LC2

FIG. 7

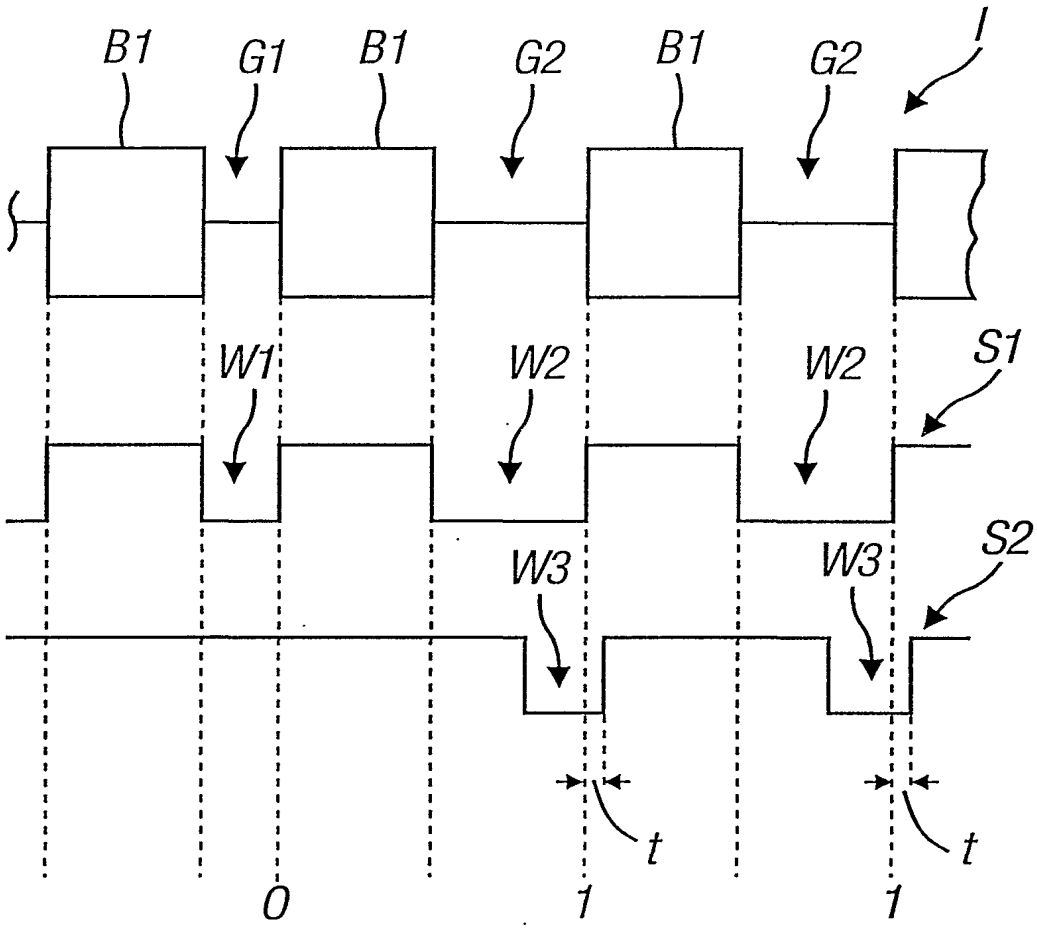


FIG. 8a

FIG. 8b

FIG. 9

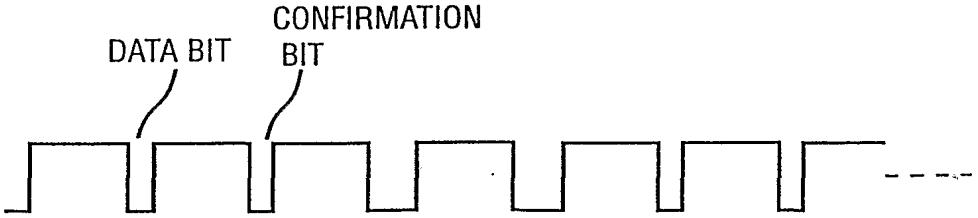


FIG. 10

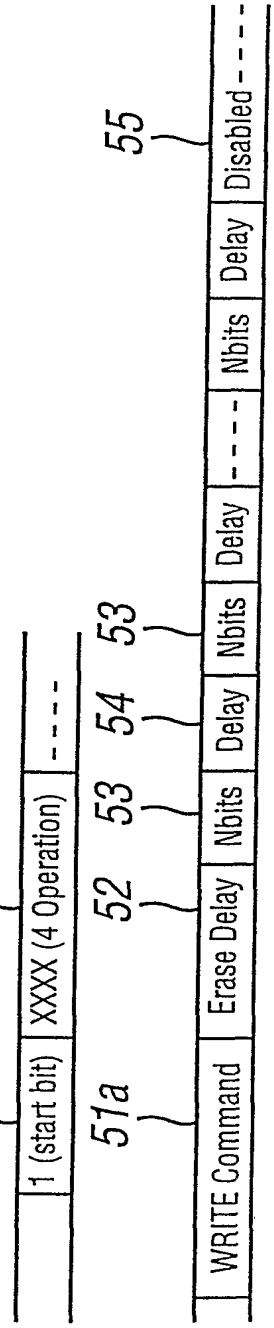


FIG. 11a

FIG. 11b

FIG. 11c

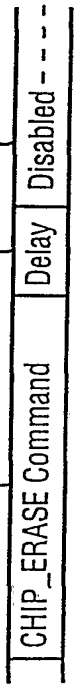


FIG. 11d

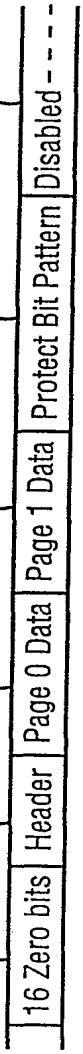


FIG. 12a

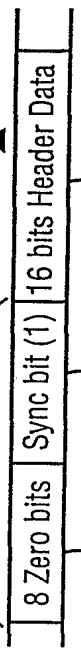


FIG. 12b

FIG. 13

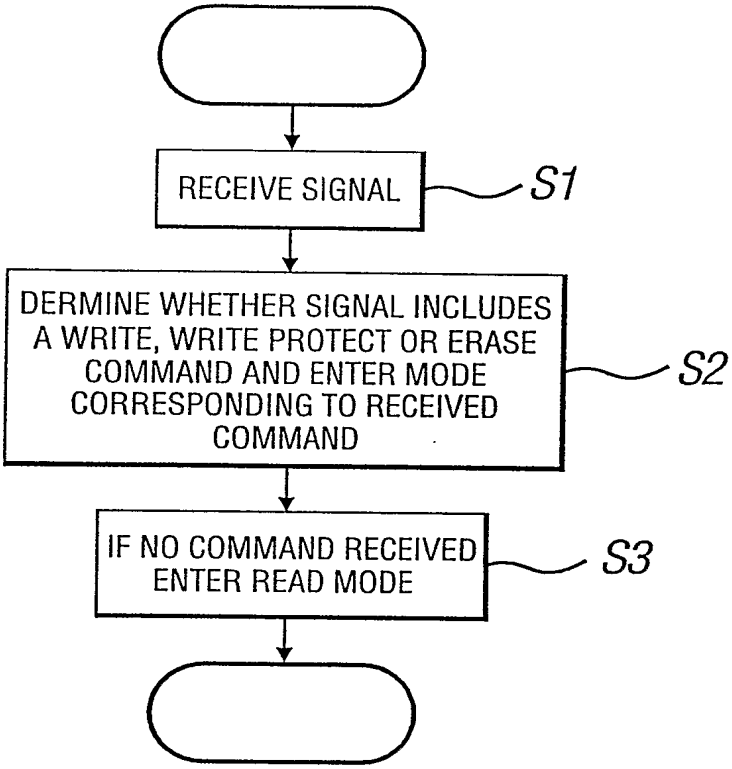


FIG. 15a

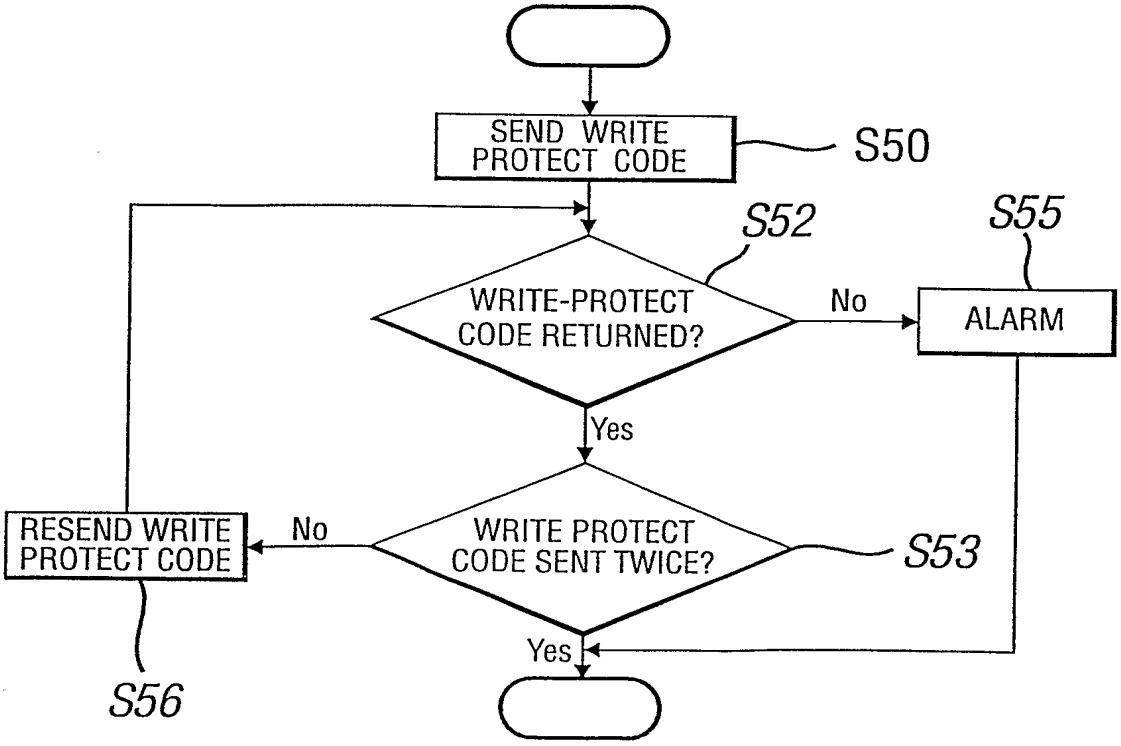
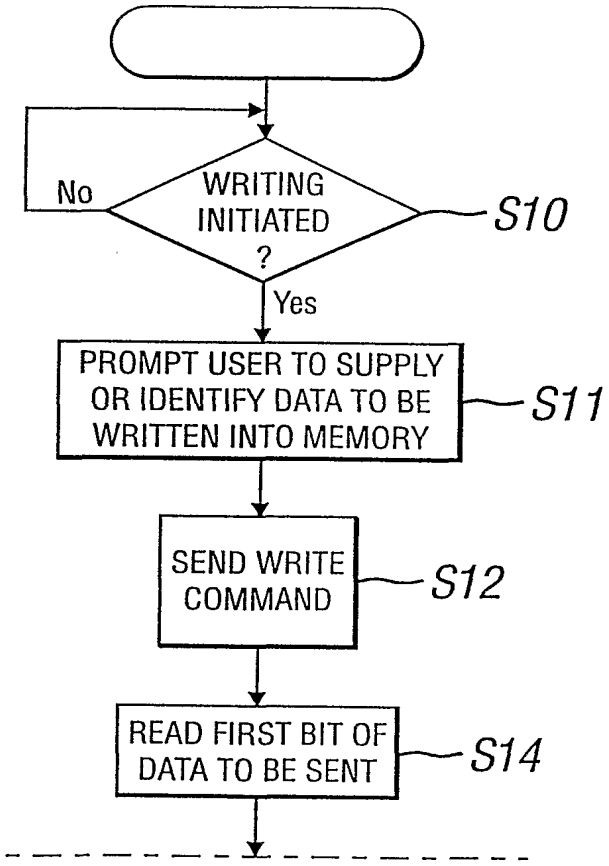


FIG. 14a


No
WRITING INITIATED ?
S10
Yes
PROMPT USER TO SUPPLY OR IDENTIFY DATA TO BE WRITTEN INTO MEMORY
S11
SEND WRITE COMMAND
S12
READ FIRST BIT OF DATA TO BE SENT
S14

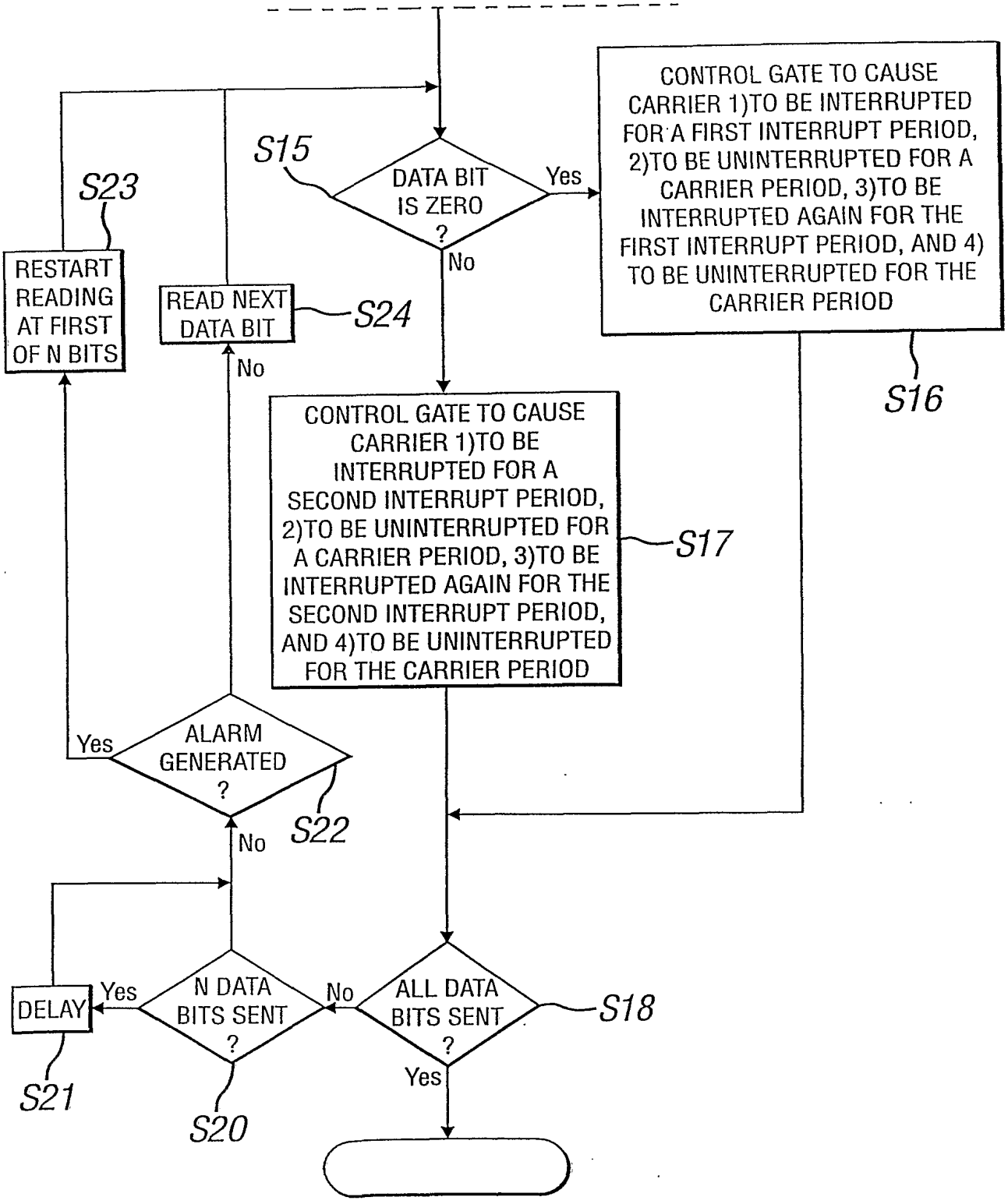

S15
DATA BIT IS ZERO ?
Yes
No
CONTROL GATE TO CAUSE CARRIER 1)TO BE INTERRUPTED FOR A FIRST INTERRUPT PERIOD, 2)TO BE UNINTERRUPTED FOR A CARRIER PERIOD, 3)TO BE INTERRUPTED AGAIN FOR THE FIRST INTERRUPT PERIOD, AND 4) TO BE UNINTERRUPTED FOR THE CARRIER PERIOD
S16
S23
RESTART READING AT FIRST OF N BITS
READ NEXT DATA BIT
S24
No
CONTROL GATE TO CAUSE CARRIER 1)TO BE INTERRUPTED FOR A SECOND INTERRUPT PERIOD, 2)TO BE UNINTERRUPTED FOR A CARRIER PERIOD, 3)TO BE INTERRUPTED AGAIN FOR THE SECOND INTERRUPT PERIOD, AND 4)TO BE UNINTERRUPTED FOR THE CARRIER PERIOD
S17
Yes
ALARM GENERATED ?
S22
No
DELAY
Yes
N DATA BITS SENT ?
No
ALL DATA BITS SENT ?
S18
Yes
S21
S20

FIG. 14b

FIG. 15b

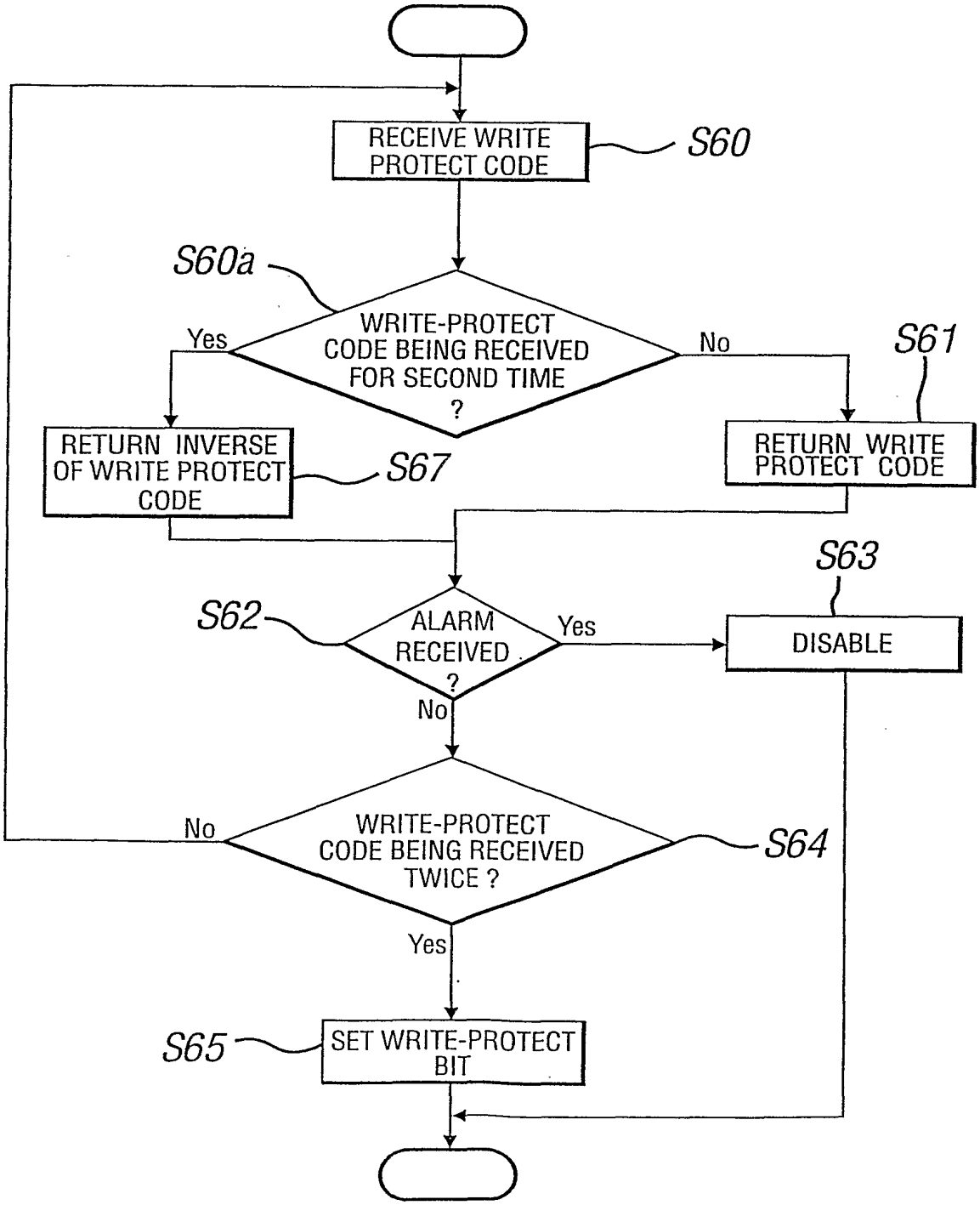

RECEIVE WRITE PROTECT CODE
S60
S60a
WRITE-PROTECT CODE BEING RECEIVED FOR SECOND TIME ?
Yes
No
S61
RETURN INVERSE OF WRITE PROTECT CODE
S67
RETURN WRITE PROTECT CODE
S63
S62
ALARM RECEIVED ?
Yes
DISABLE
No
No
WRITE-PROTECT CODE BEING RECEIVED TWICE ?
S64
Yes
S65
SET WRITE-PROTECT BIT

FIG. 16

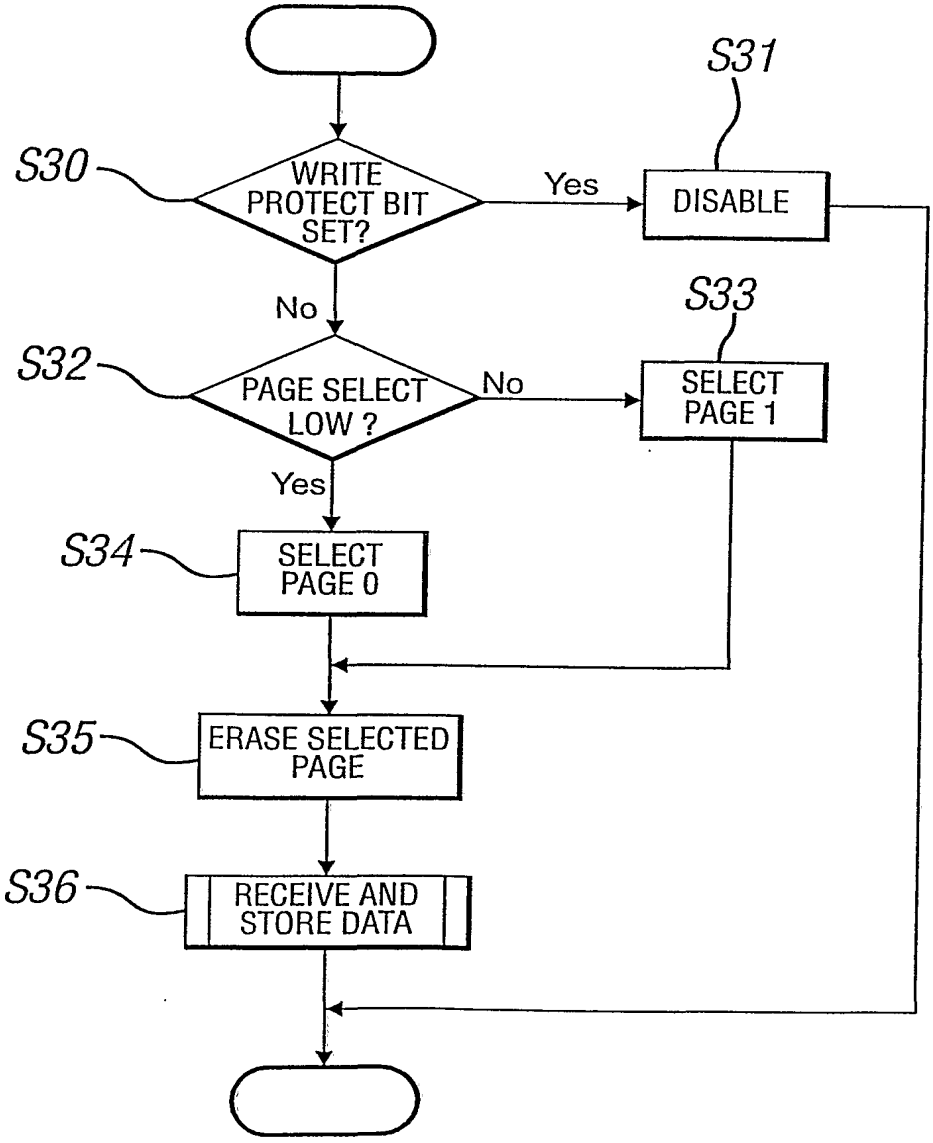

S31
S30
WRITE PROTECT BIT SET?
Yes
DISABLE
No
S33
S32
PAGE SELECT LOW ?
No
SELECT PAGE 1
Yes
S34
SELECT PAGE 0
S35
ERASE SELECTED PAGE
S36
RECEIVE AND STORE DATA

FIG. 17

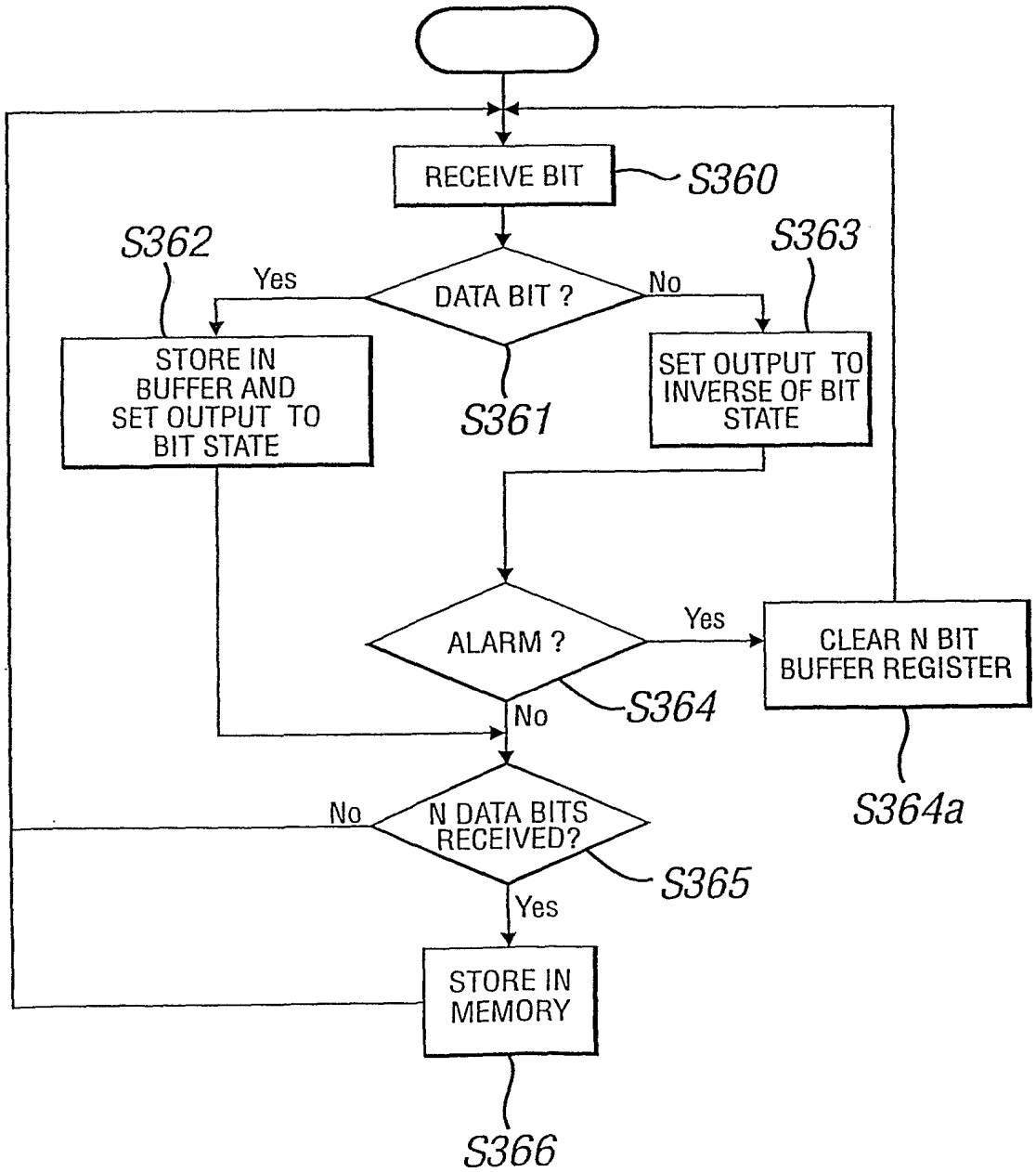

RECEIVE BIT
S360
S362
S363
Yes
DATA BIT ?
No
STORE IN BUFFER AND SET OUTPUT TO BIT STATE
S361
SET OUTPUT TO INVERSE OF BIT STATE
ALARM ?
Yes
CLEAR N BIT BUFFER REGISTER
S364
No
S364a
No
N DATA BITS RECEIVED?
S365
Yes
STORE IN MEMORY
S366

FIG. 18

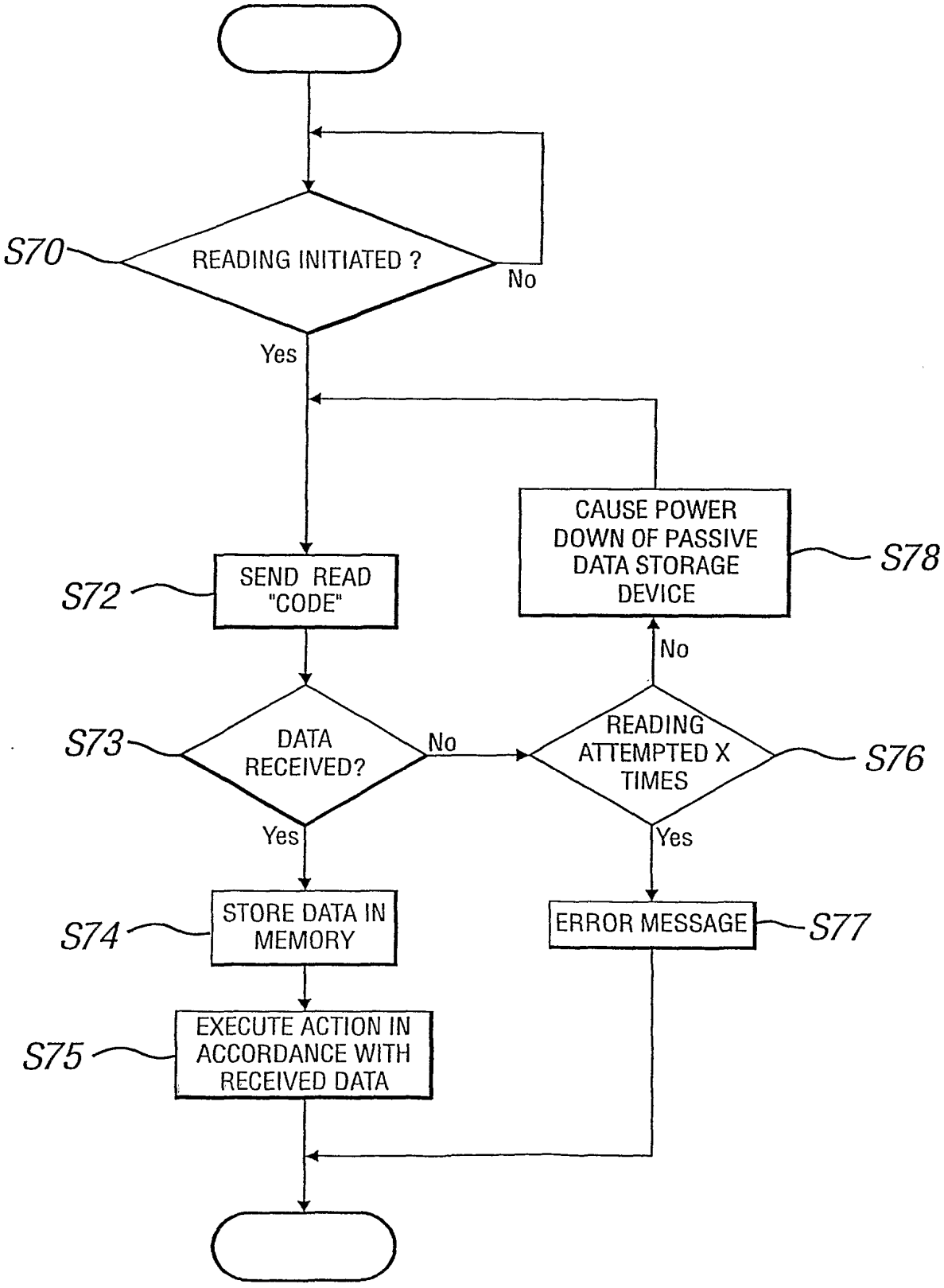

S70
READING INITIATED ?
No
Yes
S72
SEND READ "CODE"
S73
DATA RECEIVED?
No
Yes
S74
STORE DATA IN MEMORY
S75
EXECUTE ACTION IN ACCORDANCE WITH RECEIVED DATA
S76
READING ATTEMPTED X TIMES
No
Yes
S77
ERROR MESSAGE
S78
CAUSE POWER DOWN OF PASSIVE DATA STORAGE DEVICE

FIG. 21

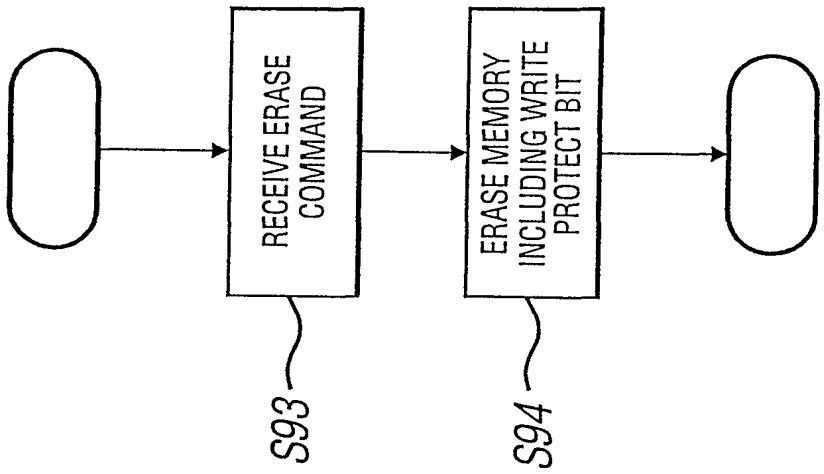


FIG. 20

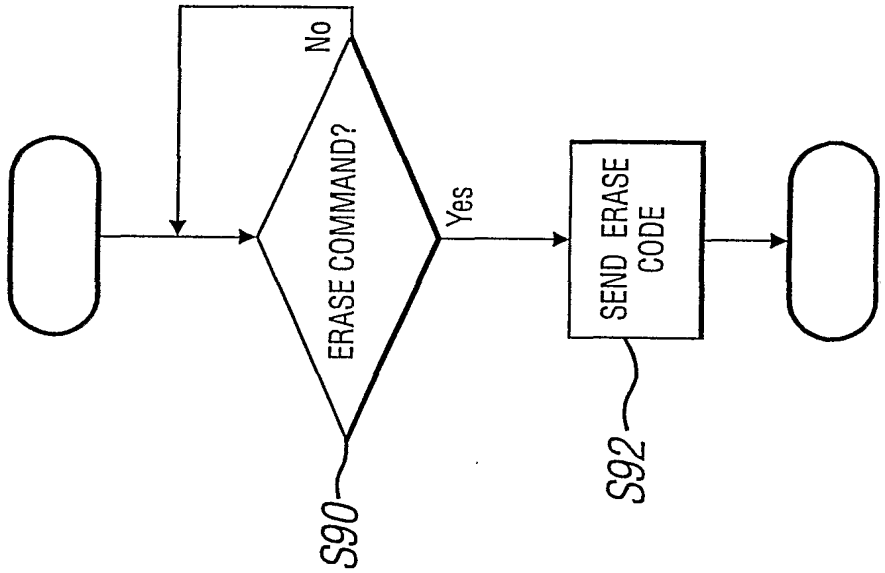


FIG. 19

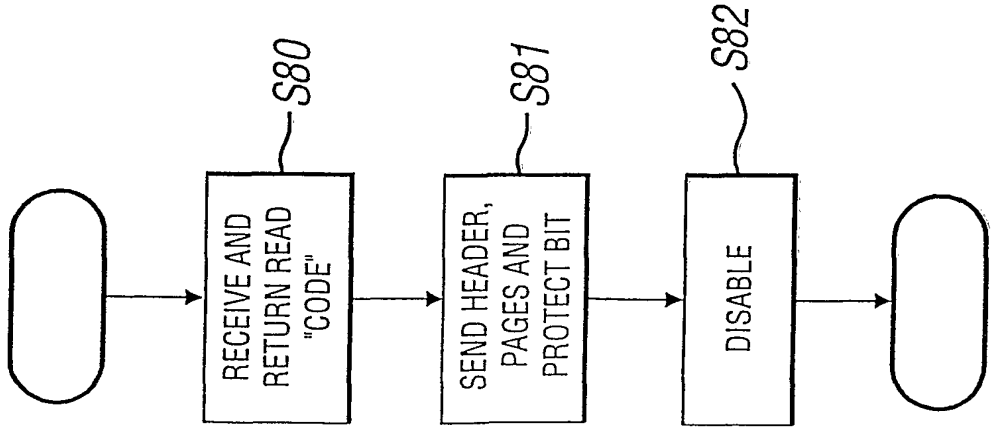


FIG. 22

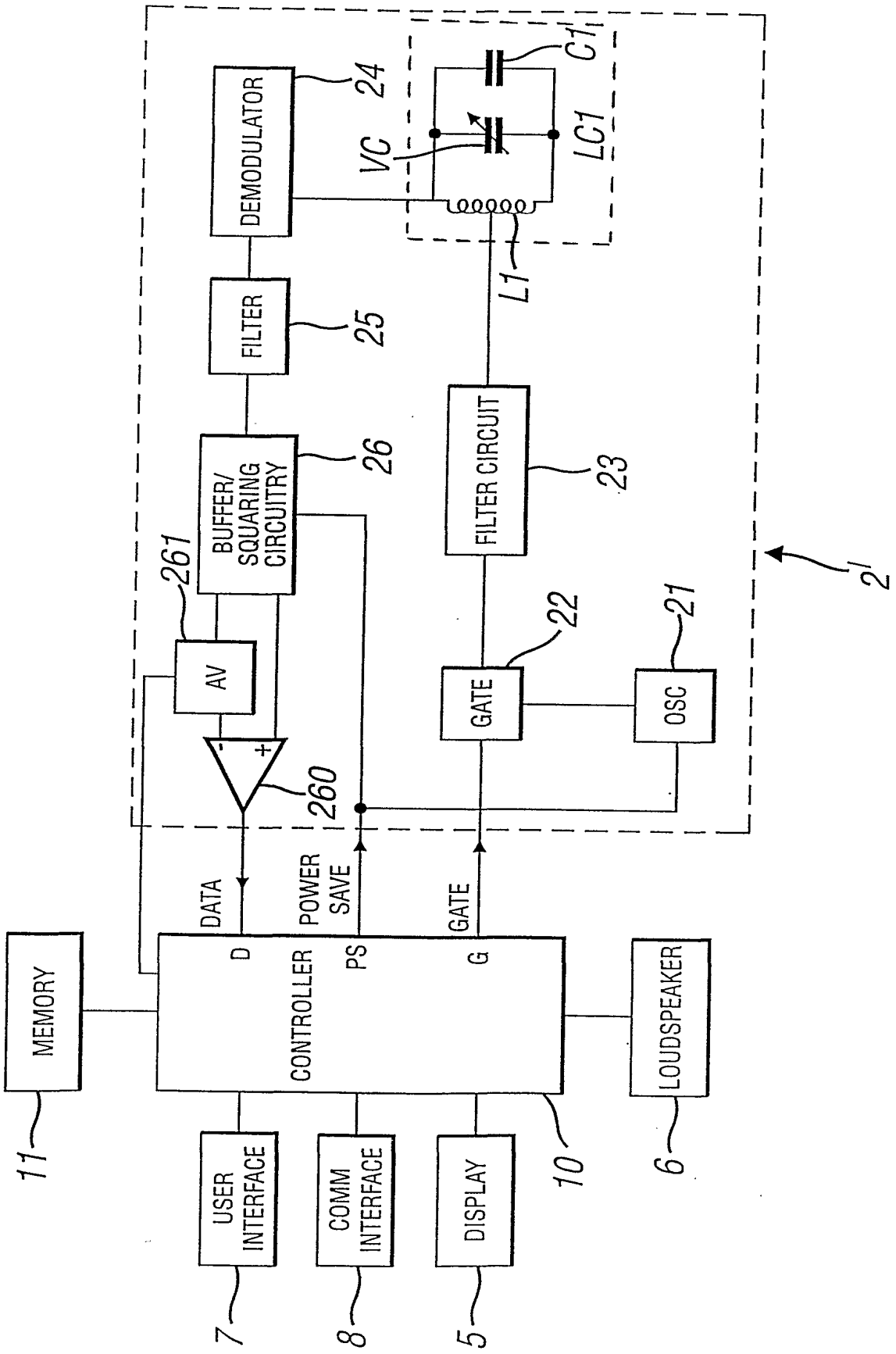
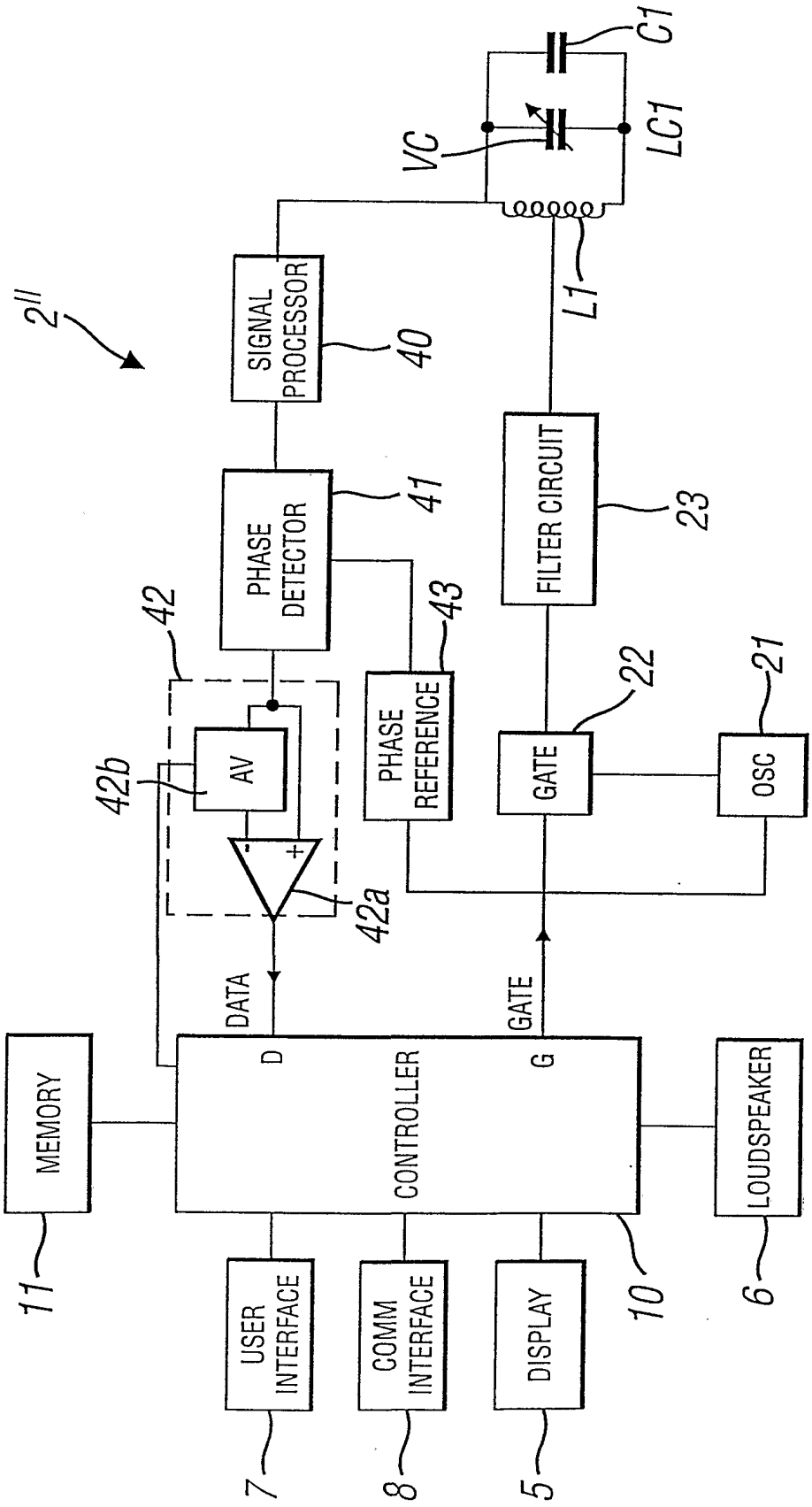

DEMODULATOR
24
VC
C1
LC1
L1
FILTER
25
BUFFER/ SQUARING CIRCUITRY
26
261
FILTER CIRCUIT
23
2
AV
GATE
22
OSC
21
260
DATA
POWER SAVE
GATE
D
PS
G
CONTROLLER
MEMORY
11
USER INTERFACE
7
COMM INTERFACE
8
DISPLAY
5
10
LOUDSPEAKER
6

FIG. 23


2II
C1
VC
LC1
L1
SIGNAL PROCESSOR
40
PHASE DETECTOR
41
FILTER CIRCUIT
23
42
43
42b
AV
PHASE REFERENCE
GATE
22
OSC
21
42a
DATA
GATE
D
G
CONTROLLER
MEMORY
11
USER INTERFACE
7
COMM INTERFACE
8
DISPLAY
5
10
LOUDSPEAKER
6

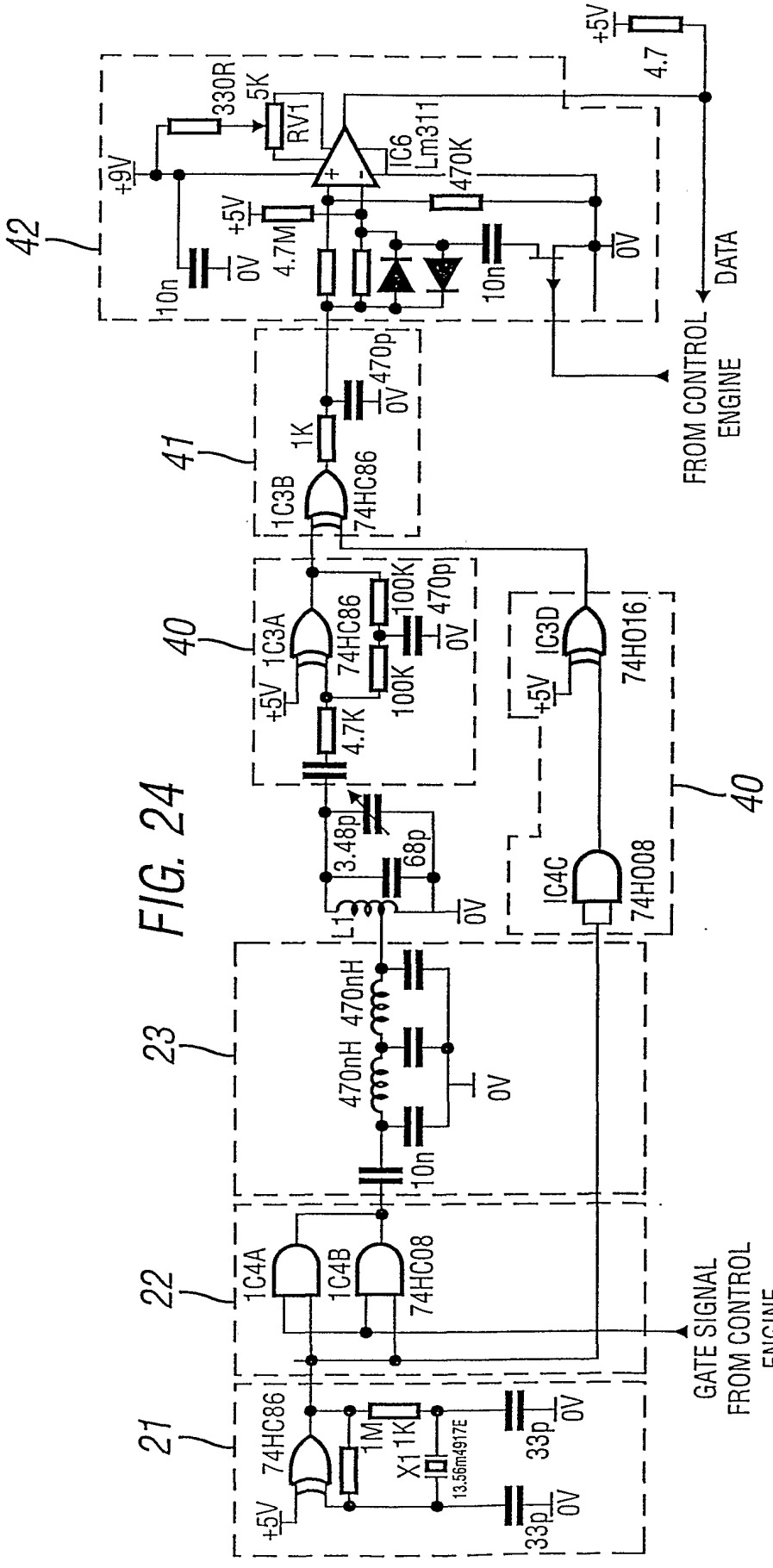
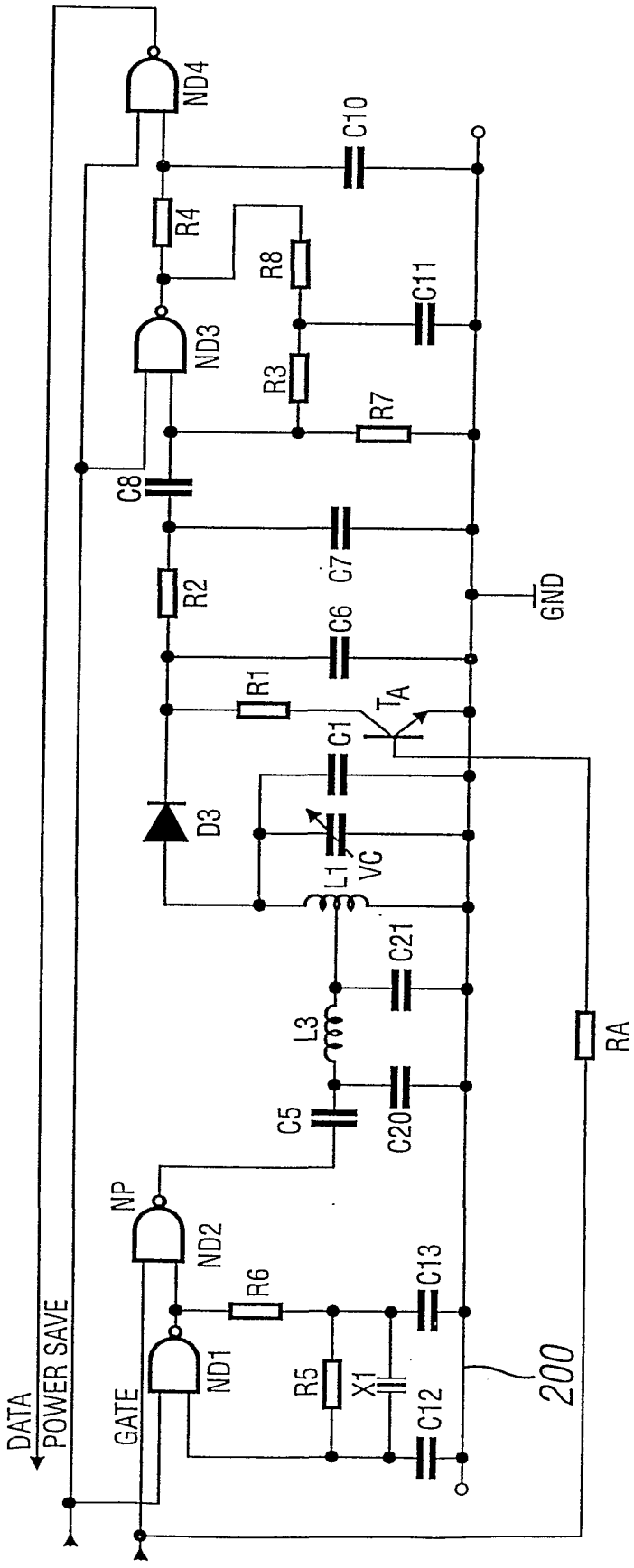

42
41
40
23
22
21
+5V
+9V
0V
330R
5K
RV1
IC6
Lm311
470K
4.7
4.7M
10n
470p
1K
1C3B
74HC86
FROM CONTROL ENGINE
DATA
1C3A
100K
4.7K
3.48p
68p
L1
IC3D
74HO16
IC4C
74HO08
470nH
1C4A
1C4B
74HC08
GATE SIGNAL FROM CONTROL ENGINE
1M
X1
13.56m4917E
33p

FIG. 24

FIG. 25


ND4
C10
R4
R8
C11
ND3
R3
R7
C8
C7
R2
GND
C6
R1
TA
C1
D3
VC
L1
C21
L3
RA
C5
C20
NP
ND2
R6
C13
ND1
R5
X1
C12
200
DATA
POWER SAVE
GATE

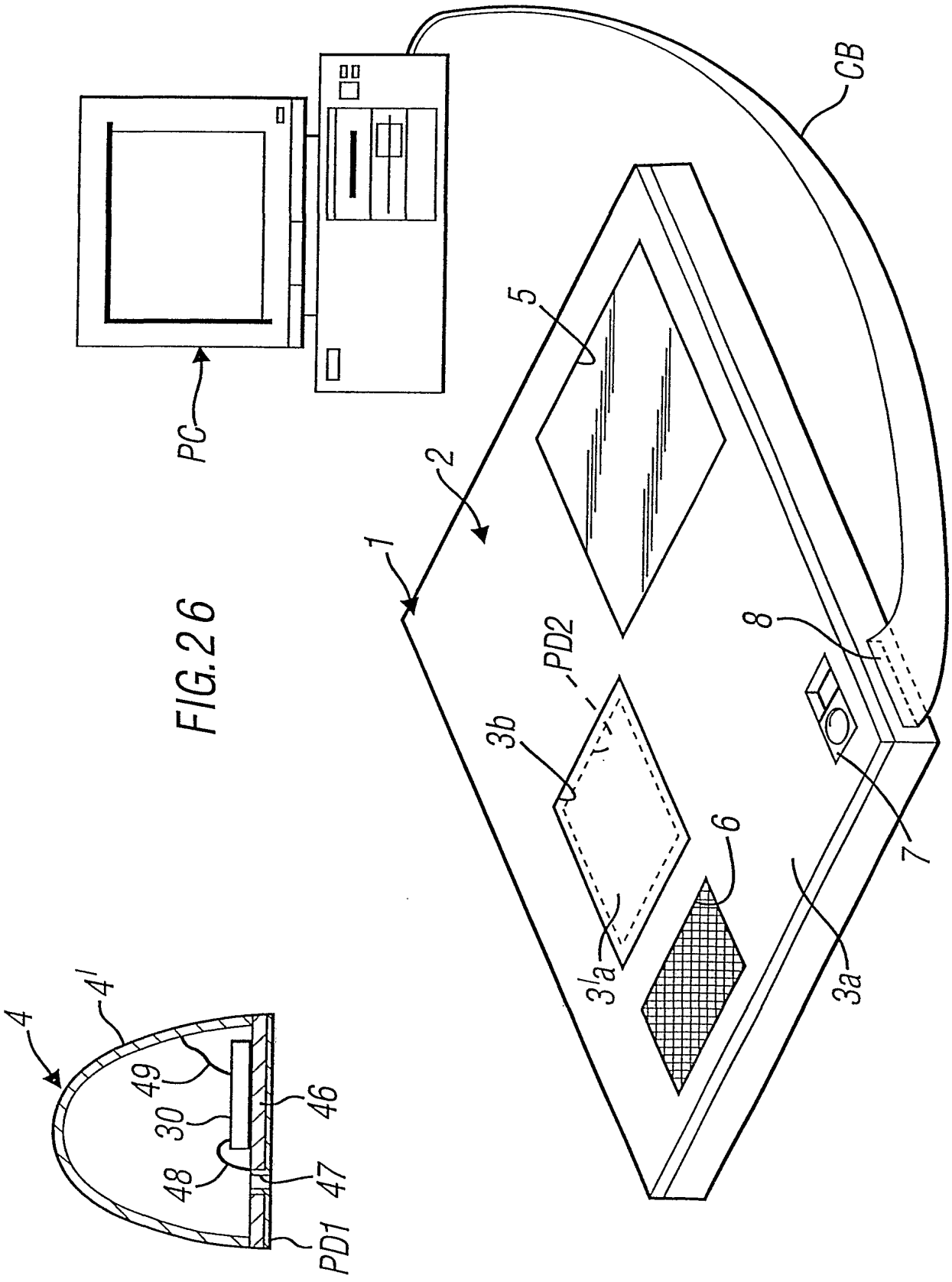


FIG.26

FIG. 27

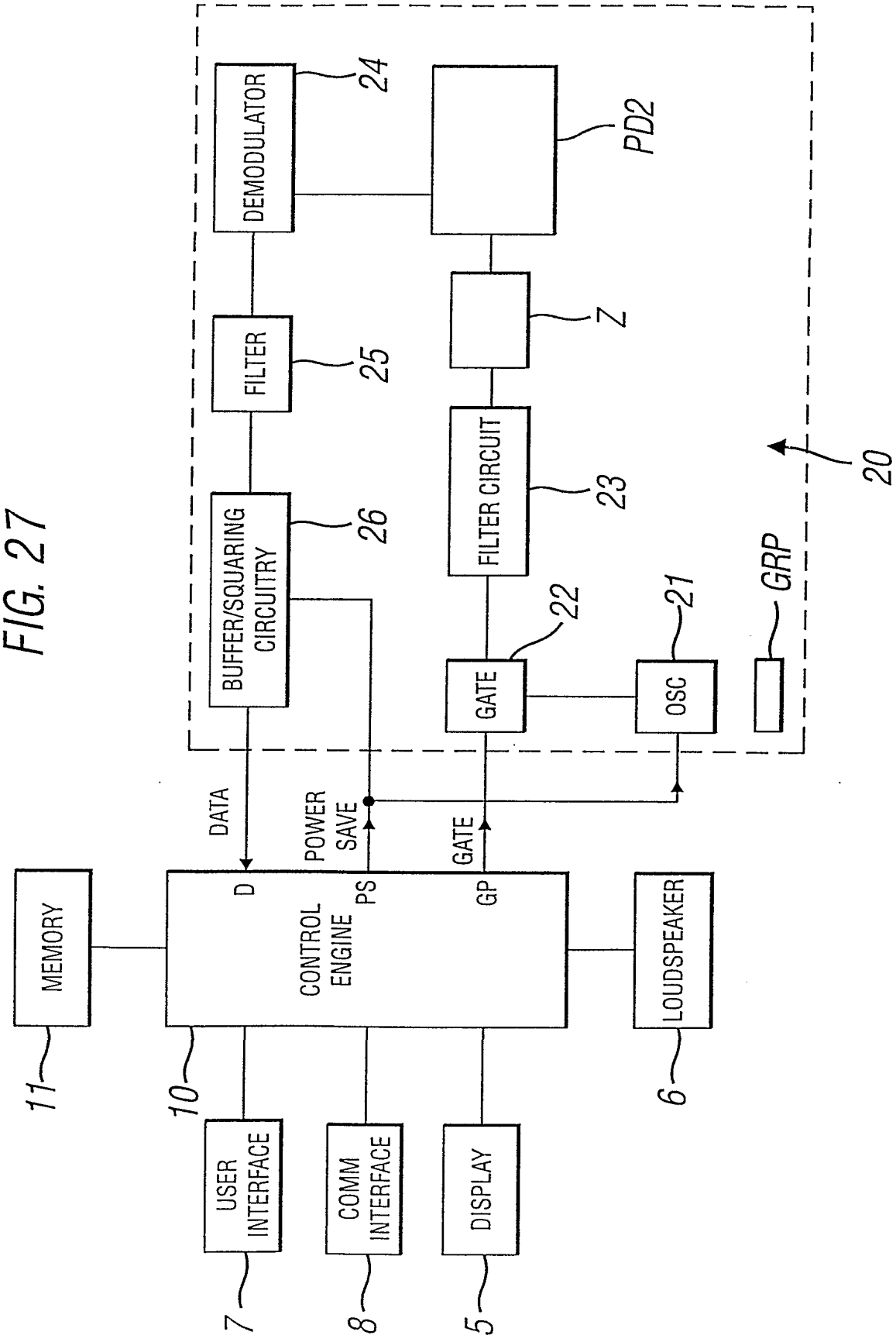

DEMODULATOR
24
PD2
FILTER
25
Z
FILTER CIRCUIT
23
BUFFER/SQUARING CIRCUITRY
26
20
GRP
21
22
GATE
OSC
DATA
POWER SAVE
GATE
D
PS
GP
CONTROL ENGINE
MEMORY
LOUDSPEAKER
11
10
6
USER INTERFACE
COMM INTERFACE
DISPLAY
7
8
5

FIG. 28

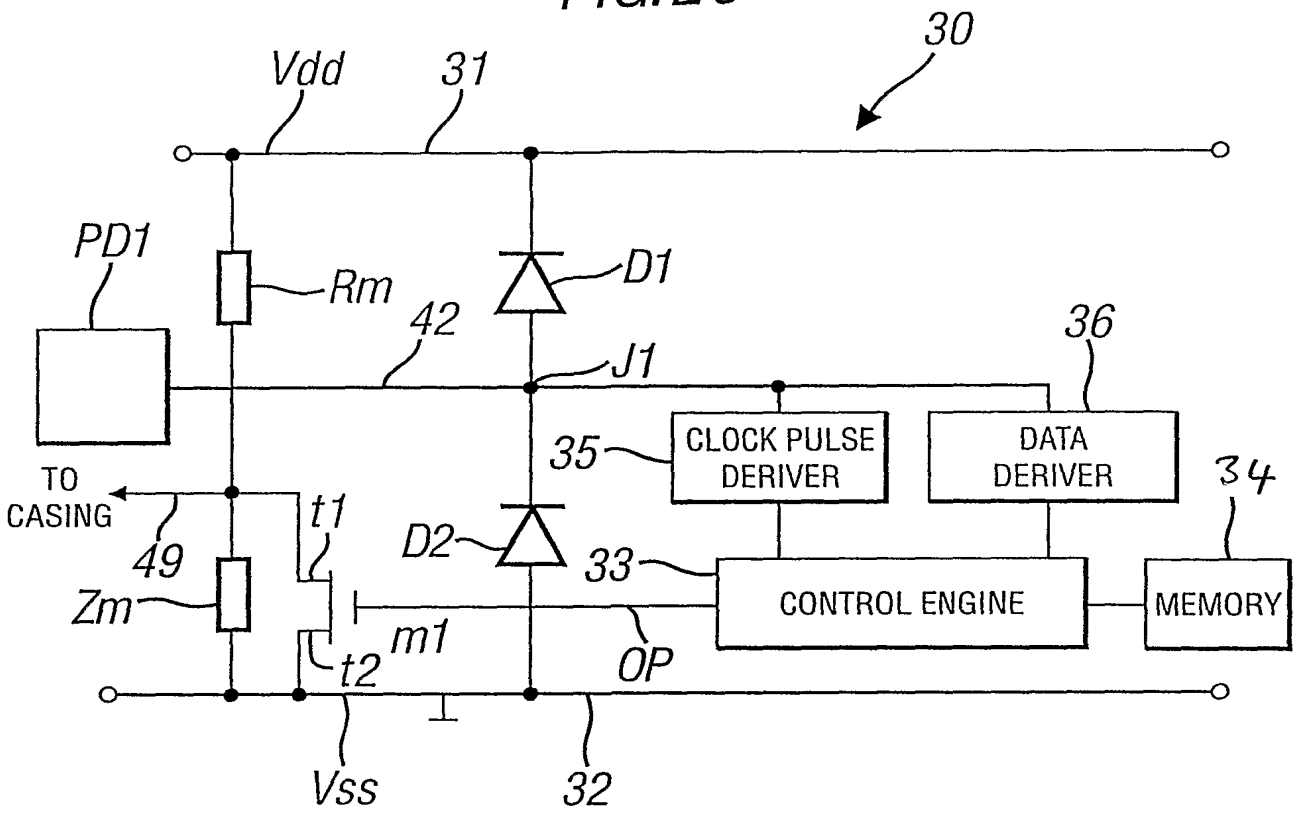

30
Vdd
31
PD1
Rm
D1
42
J1
36
35
CLOCK PULSE DERIVER
DATA DERIVER
34
TO CASING
49
t1
D2
33
CONTROL ENGINE
MEMORY
Zm
m1
OP
t2
Vss
32

FIG. 29

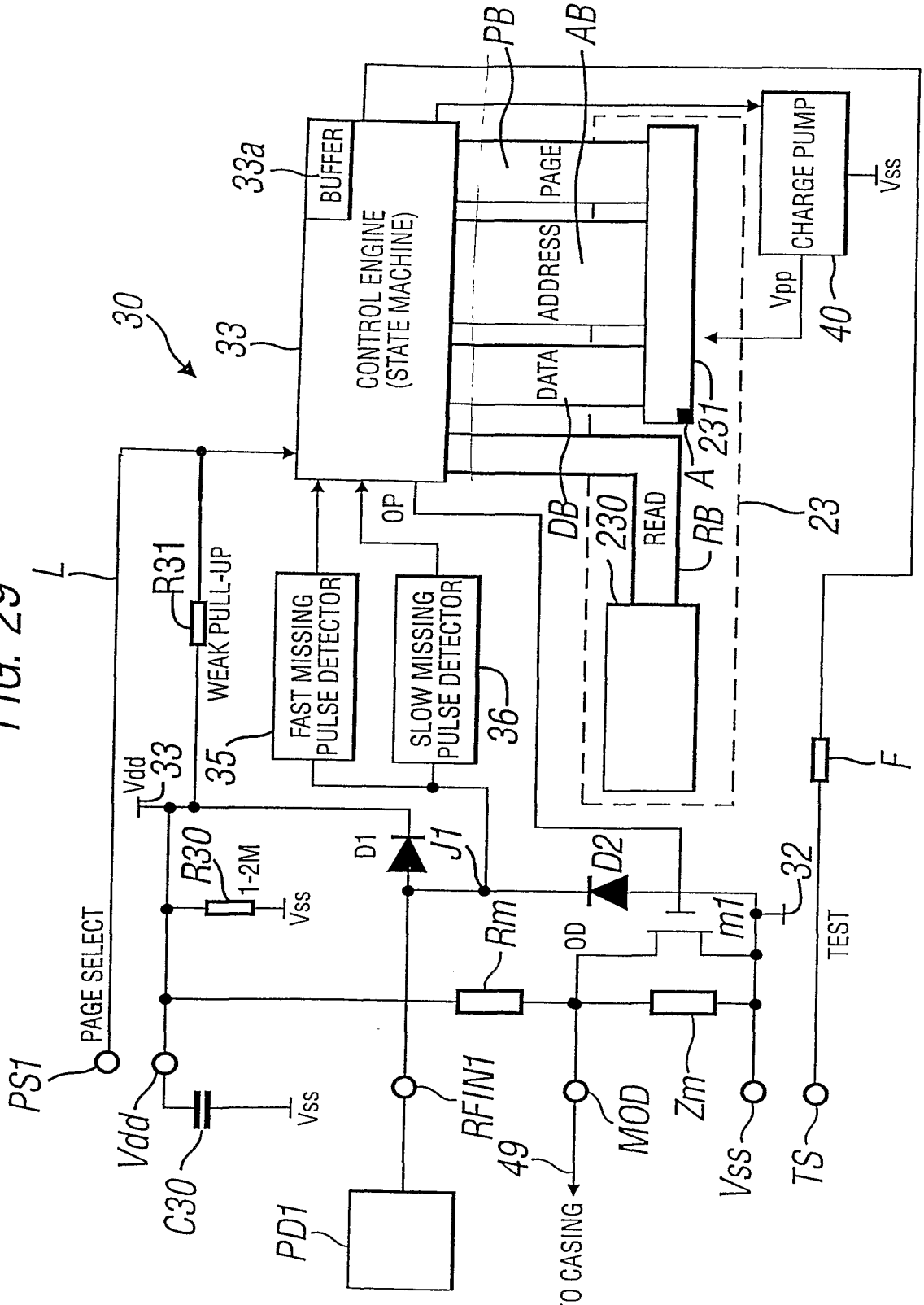
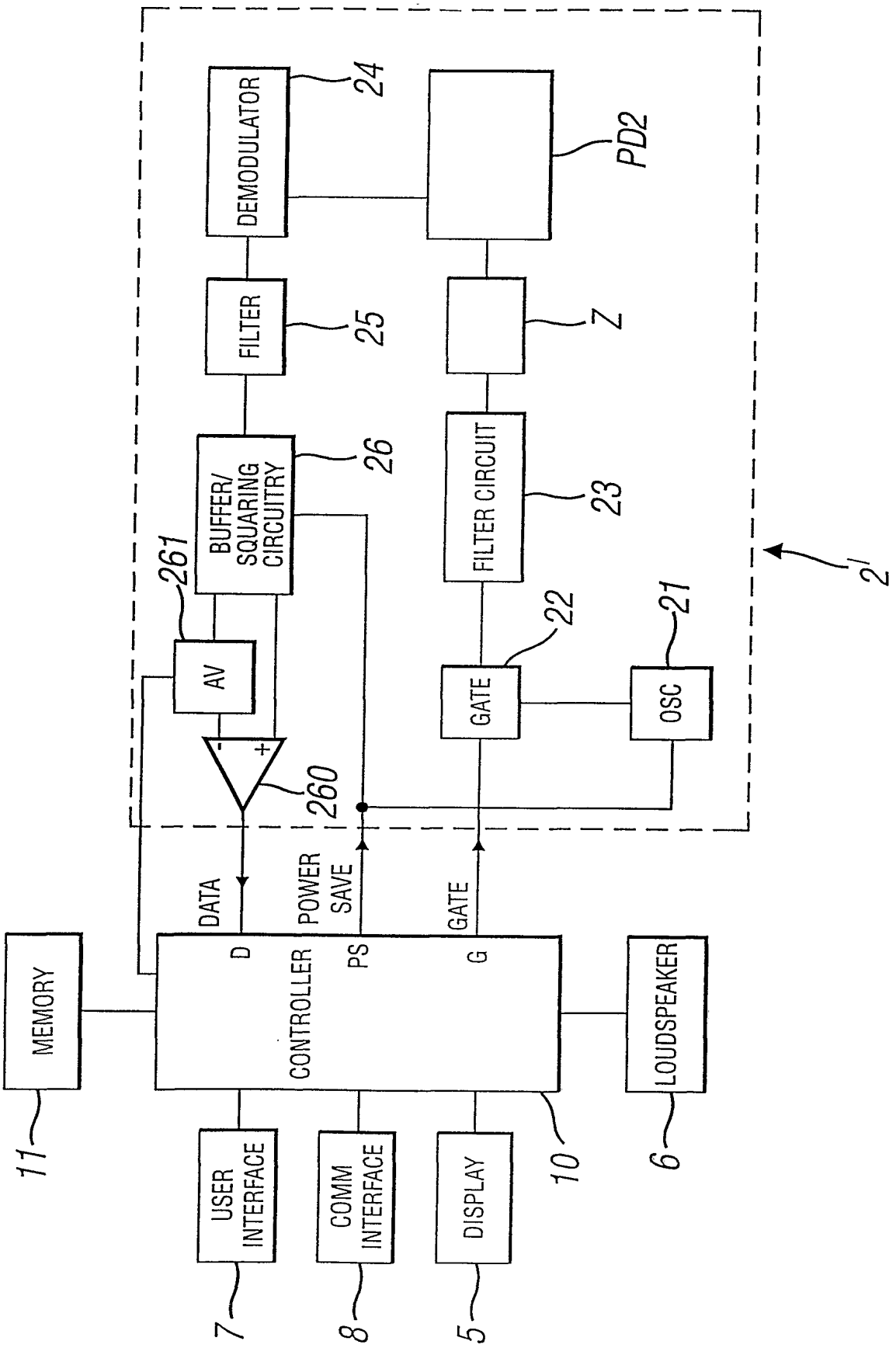

30
33
CONTROL ENGINE (STATE MACHINE)
33a
BUFFER
PB
AB
PAGE
ADDRESS
DATA
CHARGE PUMP
Vpp
Vss
40
231
A
RB
READ
230
DB
23
OP
L
R31
WEAK PULL-UP
FAST MISSING PULSE DETECTOR
35
SLOW MISSING PULSE DETECTOR
36
Vdd
33
R30
1-2M
Vss
D1
J1
D2
Rm
OD
m1
32
F
TEST
PS1
PAGE SELECT
Vdd
C30
Vss
RFIN1
49
TO CASING
MOD
Zm
Vss
TS
PD1

FIG. 30


DEMODULATOR
24
PD2
FILTER
25
Z
BUFFER/
SQUARING
CIRCUITRY
26
FILTER CIRCUIT
23
261
AV
22
21
GATE
OSC
260
2'
DATA
POWER
SAVE
GATE
D
PS
G
CONTROLLER
MEMORY
LOUDSPEAKER
USER
INTERFACE
COMM
INTERFACE
DISPLAY
11
7
8
5
10
6

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(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 July 2002 (04.07.2002)

PCT

(10) International Publication Number
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(51) International Patent Classification[7]: G06K 7/00, A63F 3/00

(21) International Application Number: PCT/GB01/05690

(22) International Filing Date:
20 December 2001 (20.12.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

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0031553.1	22 December 2000 (22.12.2000)	GB
0031533.3	22 December 2000 (22.12.2000)	GB
0031577.0	22 December 2000 (22.12.2000)	GB
0031575.4	22 December 2000 (22.12.2000)	GB
0031520.0	22 December 2000 (22.12.2000)	GB
0031530.9	22 December 2000 (22.12.2000)	GB
0031516.8	22 December 2000 (22.12.2000)	GB
0031544.0	22 December 2000 (22.12.2000)	GB
0031541.6	22 December 2000 (22.12.2000)	GB

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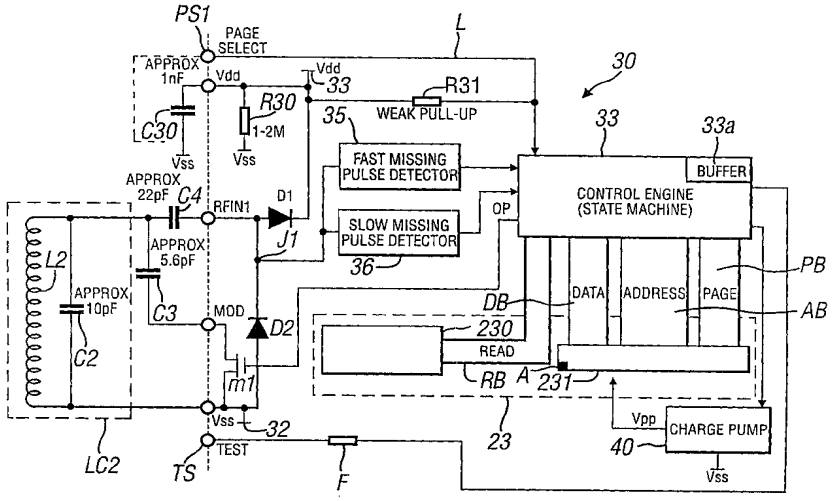
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,

[Continued on next page]

(54) Title: DATA COMMUNICATION APPARATUS



(57) Abstract: A base module (2) has a subsidiary unit receiving area (3b) having a first electrical coupler (LC1). A subsidiary unit (4) has a memory (231) and a second electrical coupler (LC2) arranged to couple to the first electrical coupler when the subsidiary unit is received on the subsidiary unit receiving area (3b). The base module (2) has a signal supplier (10, 21) for supplying a signal to the subsidiary unit (4) when the first and second electrical couplers (LC1 and LC2) are coupled and a data communicator (10, 22) for interrupting the signal in accordance with data to be communicated to the subsidiary unit to provide to the first coupler (LC1) an interrupted signal having interruptions dependent upon the data to be communicated. The data communicator is arranged to send the data as data bits each followed by a confirmation bit and the subsidiary unit has a data returner (33, M1) for modifying the received signal to return the received data as it is received so that each returned data bit is followed by the inverse of the corresponding confirmation bit.

WO 02/052419 A3

CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 01/05690

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06K7/00 A63F3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06K A63F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
WPI Data, PAJ, IBM-TDB, INSPEC, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB 2 344 257 A (INNOVISION RESEARCH AND TECHNO) 31 May 2000 (2000-05-31) abstract; claims 1-7; figures 1,3	1,11,12, 38-42, 51,52
A	WO 97 23060 A (BORRETT MARC ADRIAN ;INNOVISION RES & TECH LTD (GB); WHITE ANDREW) 26 June 1997 (1997-06-26) abstract; figure 1	1,11,12, 38-42, 51,52

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 March 2002	01 07 2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	CHIARIZIA, S

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 01/05690

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KARDEL: "DTS/NTP Zeitsynchronisationsverfahren in verteilten Systemen" November 1993 (1993-11) , INSTITUT FÜR MATHEMATISCHE MASCHINEN UND DATENVERARBEITUNG DER FRIEDRICH-ALEXANDER-UNIVERSITÄT ERLANGEN-NÜRNBERG , NÜRNBERG XP002194517 page 5, line 4 - line 7 -----	1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB 01/05690

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-24, 27-42, 51, 52,

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-24,27-42,51,52

Data communication apparatus comprising a base module and a subsidiary unit, the base module comprising communication means being arranged to send data bits each followed by a confirmation bit and the subsidiary unit having data returning means for returning the data as it is received followed by the inverse of the corresponding confirmation bit.

2. Claims: 25-42,51,52

Data communication apparatus comprising a base module and a subsidiary unit, the subsidiary unit comprising at least two memory areas, area selecting means that are preset and encapsulated.

3. Claims: 43-50,52

Data communication apparatus comprising a base module having signal supplying means and first electrical coupling means for coupling to second electrical coupling means of a subsidiary unit, the base module comprising control means to control whether or not the signal supplied by the supplying means is supplied to the first electrical coupling means

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 01/05690

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2344257 A	31-05-2000	AU 1287400 A	13-06-2000
		EP 1145183 A1	17-10-2001
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